

Features

- Exact replacement of existing Altera 7000 CPLDs.
- 10 week lead time for production quantities.
- NRE amortized over production.
- Identical package footprint means no board redesign
- Easy engineering interface. We work from your existing files.
- Automatic Test Program Generation (ATPG)
- Small or large production quantities supported.

Major Customer Benefits

- Reduce long leadtimes on Altera 7000 series CPLDs by up to 50%.
- Save 50% or more on cost of CPLDs
- Solve product obsolescence issues
- Guaranteed to work – no risk
- Fast turnaround on most CPLD replacements

CPLD Conversions

CPLD conversions consist of reimplementing an CPLD design into an ASIC. There are a number of reasons to convert a design. An ASIC will have lower unit cost, lower power, higher performance, and more package flexibility. These benefits have to be weighed against the NRE charges, and the lack of reprogrammability.

Tekmos provides customers with comprehensive engineering support. We accept designs on an "as is" basis, translate them into our internal cell libraries, and perform the engineering work necessary for a successful conversion.

Production volumes of ASICs are generally available 10 weeks after receipt of order.

CPLD Conversion Flow

Tekmos accepts designs in any format. Most designs arrive as CPLD netlists. We also convert HDL netlists.

CPLD Conversion

We request that the customer provide us with the original design files, along with any simulations that may exist. We can accept either pre-synthesis RTL level designs, or gate level designs.

We also request two pre-programmed parts. Tekmos uses these parts to verify the design by comparing the simulated performance against actual results derived from the CPLD.

Simulations and Sign-Off

Original simulations (if they exist) will be enhanced with Tekmos generated simulations and used for production testing.

Replacing an CPLD means that Tekmos is responsible for the post-route signoff. Customer participation, while optional, is encouraged.

Prototypes

The design will be fabricated, assembled, and tested. Prototypes are available in about 8 weeks after tape-out.

Quotations

Within a given CPLD, the size of the individual CPLD design can vary considerably, depending on the number of gates, the amount of memory, and the number of used pins. On the other hand, the cost of the ASIC replacement is directly linked to the design size. That is why we need to review the design netlist to provide an exact quotation.

Tekmos can provide a budgetary quotation based on the full CPLD part number and desired annual volume. A more accurate budgetary quotation can be obtained if the CPLD utilization report is provided. Tekmos offers quick turn ASIC replacements of many other CPLDs and FPGAs upon request.

**NREs
(Non-Recurring Engineering)**

Converting a CPLD into an ASIC involves engineering work, a dedicated mask set, and test hardware. The NREs may be amortized over the first six months of production, or may be invoiced directly when the customer does not wish to commit to production volumes.

Speed Grades

Altera provides a speed grade sort for their products. The number corresponds to the propagation delay through the part. It also corresponds to a maximum clock speed for internal logic.

The design of the Altera 7000A and AE families is optimized for maximum performance in the propagation delay. In general, the propagation performance of the Tekmos arrays is equivalent to a -10 rating by Altera.

The maximum internal array clock speed is another matter. Tekmos devices can easily support the -7 speeds, and operation at the -4 and -5 speeds can be achieved depending on the individual circuit design.

Altera's Maximum Clock Frequency (MHz)

| Device | -4 | -5 | -7 | -10 | -12 |
|--------|-----|-----|-----|-----|-----|
| 7032AE | 227 | | 139 | 103 | |
| 7064AE | 222 | | 135 | 100 | |
| 7128AE | | 192 | 130 | 98 | |
| 7256AE | | 172 | 127 | 95 | |
| 7512AE | | | 116 | 87 | 72 |

Packaging

Tekmos can match the original Altera packaging. However, some packages are nearly obsolete, and their use may impact the leadtimes.

In general, TQFP packages have the best availability. BGAs may require additional time due to substrate availability. And the 84 pin PLCC is becoming difficult to obtain.

Lead Times

Our 10 week lead time can be divided into four steps. Here is how it breaks down.

Design Conversion – 2 weeks

We have to re-implement each design in our library. While the actual conversion is straight forward, we then have to analyze whether or not the conversion has introduced a race condition that might kill the chip. We also have to develop test vectors that will exercise the design well enough to allow it to be tested in a production environment.

Then the design goes to layout. When done, it must be re-checked to verify that the routing has not introduced any new problems.

The entire design phase typically takes two weeks. A difficult design can take up to four weeks. A straight-forward design with vectors can take one week.

Wafer Fabrication- 4 weeks

The next step is to generate photomasks. That takes a week. Then, it takes three additional weeks to process the wafers from contacts onwards. The last step is to ship the wafers to the assembly house.

Assembly – 3 weeks

Package assembly is one of the biggest variables in the lead time. Tekmos uses three different assemblers, depending on the package type. The turn-time can range from 1.5 weeks up to 4 weeks. The shipping back to the Tekmos factory will vary from 1 to 4 days, depending on the assembler location.

Final Test – 1 week

Tekmos does the testing at our facility. Generally, testing is done on the same day as the parts are received. The dehydration bake takes another day. Then prototypes are shipped to the customer.

Production

Tekmos builds the initial production quantities along with the prototypes. That allows us to release production quantities as soon as prototypes are approved.

Depending on the package and volumes, a few extra days may be needed to complete testing, lead scan, and optionally tape and reel.

Expedites

Expedites are available. Our wafer foundry accepts “bullet lots”, which can save up to two weeks. Depending on the assembly houses, “hot lots” are available that can reduce the turn times down to about one week. Overall, the best that can be done is to reduce the lead time to about 5 weeks.

Expedites carry a good deal of risk, mainly relating to missed schedules. Still, that can be useful in a lines-down situation.

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Revision History

| Date | Revision | Description |
|---------|----------|-----------------|
| 7/21/10 | 1.0 | Initial release |

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