

Features

- Bitstream-based conversion service
- Supports designs with lost or questionable source code
- Pin-for-pin FPGA replacement
- Supports Multiple FPGA Families
 - Xilinx 3000 Series
 - Xilinx 3000A Series
 - Xilinx 3000L Series
 - Xilinx 4000 Series
 - Xilinx 4000A Series
 - Xilinx 4000E Series
 - Xilinx 4000EX Series
 - Xilinx 4000XL Series
 - Xilinx 4000XLA Series
- JTAG support (optional)
- Program load emulation (optional)
- No-NRE charges
- Test vectors are not required
- 1000 unit minimum order quantity
- No risk conversion
- Low cost

Introduction

FPGAs are an excellent solution for many systems. However, they all have a potential documentation problem, since the design source code is separate from the bitstream used for manufacturing.

It is all too common for the manufacturing version of the design source code to become lost. Last minute design changes may not have been filed with document control. Companies are reorganized, people leave, and then 10 years later, no one can find the original design.

This is not a problem as long as the original FPGA is available, and there is no need to change the design. However, when the FPGA is obsoleted, or the end product comes under cost pressure, then the lack of design source code becomes a big problem.

The Tekmos EasyWire program is your solution. Starting with just the FPGA programming bitstream, Tekmos provides ASICs that are pin-for-pin compatible with the original FPGA.

EasyWire FPGA Replacements

The preferred approach to replacing an obsolete FPGA with an ASIC is to start with the original design files, and re-synthesize them into a newer technology. But this is not possible when the original design files are lost.

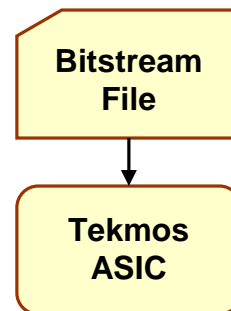
With the Tekmos EasyWire program, the conversion process begins with the bitstream file used to program the original FPGA. Nothing else is required.

As a first step, Tekmos converts the raw bitstream file into a Verilog netlist. This initial netlist is complete, but is not in a usable format. It is post-processed and optimized to remove unneeded logic, and to turn it into a form suitable for implementation as an ASIC.

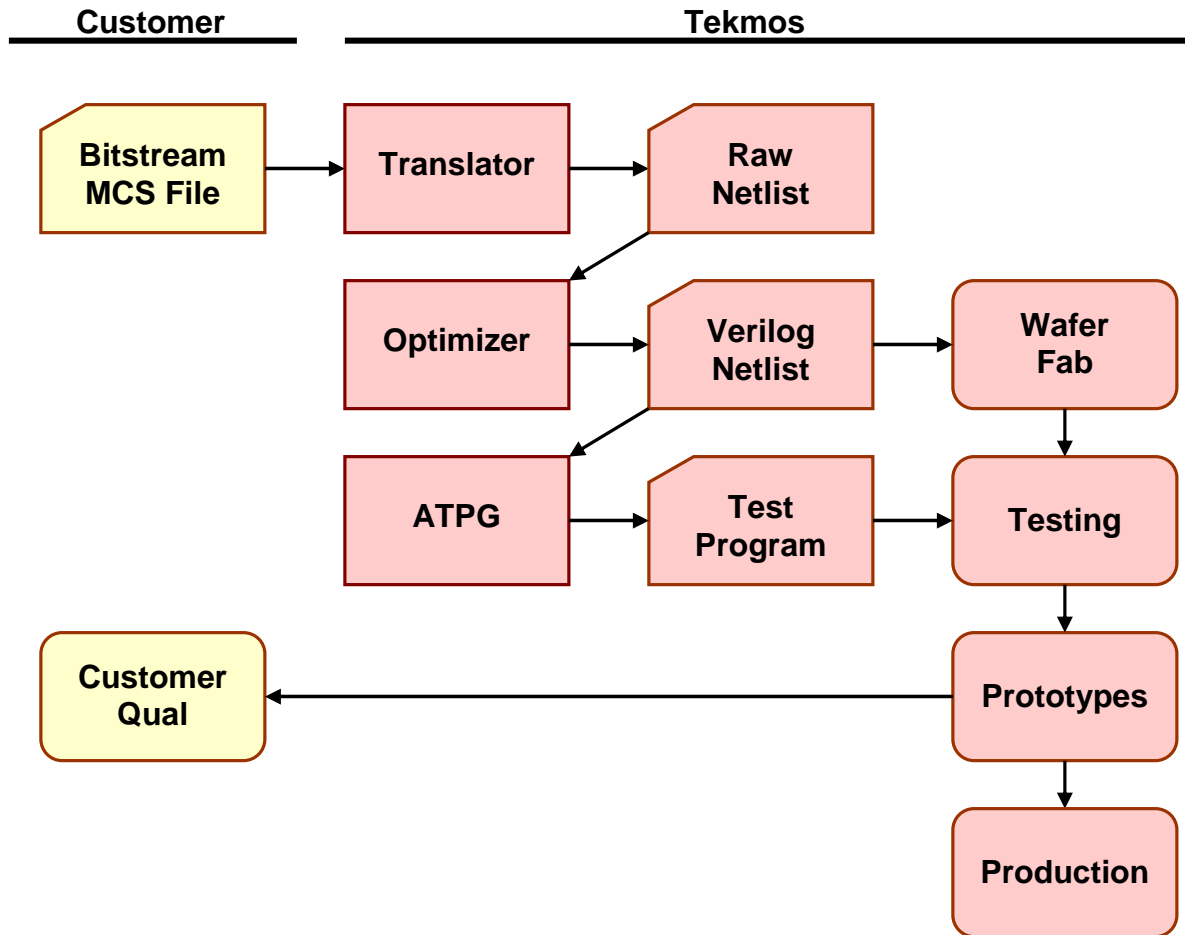
Once the final netlist is available, it is implemented as an ASIC, using the Tekmos Merged ASIC Program (MAP). At this point, it becomes a manufacturable part and normal manufacturing flows apply.

In parallel, test vectors are generated through the use of our ATPG software. These vectors are used to test the parts prior to delivery.

The Tekmos EasyWire ASIC is not an FPGA. And each conversion involves multiple technical issues, which are covered in this data sheet. Even so, the EasyWire conversion uses less customer resources than it would take to re-design the original circuit.



**Tekmos EasyWire
FPGA Conversions**



Program Load Emulation

The Tekmos EasyWire ASIC provides program load emulation as an option. Some customers may wish to achieve cost savings by removing the FPGA program storage from their system. Other customers may be using a microprocessor to initialize the FPGA, and their system software requires the handshaking to perform correctly. Tekmos allows the customer to specify the initialization sequence.

Since the EasyWire part is an ASIC, it will accept the program data, and then ignore it. The EasyWire part with program load emulation will operate correctly in a daisy-chain programming configuration.

JTAG Support

The Tekmos EasyWire ASIC provides emulation of the FPGA JTAG circuitry. JTAG support can be added to designs that did not have it originally, or used it only as a special program during board test.

Conversion Issues

The EasyWire program produces an ASIC. It is not an FPGA. It will most likely be implemented in a newer technology. It uses gates rather than look-up tables, and it has different timing.

Tekmos analyzes each design before we implement it. But this is a difficult task when dealing with re-generated designs. Particularly, if the original design relies on routing dependent timing for correct operation, then the ASIC implementation may not work the first time. This is why Tekmos offers a no-risk guarantee on our conversions.

No Risk Conversion

Tekmos guarantees that the EasyWire replacement will work in the customer's system. If it does not work, we will correct, at our cost, any problems identified by the customer and generate new prototypes.

Problem Designs

Occasionally, designs will require extra attention. This may be due to critical system timing, or other issues that the customer is aware of. In these cases, Tekmos can provide an extra level of engineering support, including characterization of the original part performance, and the generation of manual test vectors.

Original Design Ownership

Tekmos requires all customers of the EasyWire program to certify that they have the legal rights to the design we are converting.

Implementation

Tekmos implements the netlist produced by the EasyWire program as an ASIC. Depending on the circuit size and package type, we merge the design with other designs, and make ASIC prototypes. After customer approval, production can begin.

I/O Characteristics

DC I/O characteristics are set to the same values as found in the original FPGAs. Other values are available upon request.

Test Vectors

Tekmos uses ATPG software to generate scan vectors for the design. The scan test mode is transparent to the customer in normal device operation.

Tekmos makes use of a proprietary scan technique that minimizes the effects of scan insertion on internal timing.

No NRE Charges

Normal ASIC NRE charges are waived, in lieu of a production order for a minimum of 1000 units, conditional on prototype approval.

Prototype Approval

Tekmos will provide 10 prototypes for customer approval. The delivery of the balance of the order will be scheduled after prototype approval has been obtained.

Because of the batch processing used in semiconductor manufacturing, Tekmos can frequently meet the initial production requirements within 4 weeks. Normal production lead times will apply to subsequent orders.

Contact Information

EasyWire FPGA replacements may be ordered directly from Tekmos

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Revision History

Date	Revision	Description
2/24/05	1.0	Initial Release

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