Tekmos

TK80C186EB / TK80C188EB Microprocessors

(V1.3) April 5, 2010 — Product Overview

Features

- o Static 186 CPU core.
- o Idle and Powerdown Modes
- o Clock Generator
- o 2 Serial Channels with Independent Baud Rate Generators
- o 3 Programmable 16-Bit Timers
- o 2 Parallel Ports
- o 10 Programmable Chip Selects with Programmable Wait State Generators
- o Memory Refresh Generator
- o High Impedance Test Mode (ONCE)
- o High Speed Operation
  - 25 MHz @ 5 V
  - 16 MHz @ 3 V
- o 1 MB Memory Address Capability
- o 64 KB I/O Address Capability
- o Available in the Following Packages:
  - 84 Pin PLCC
  - 80 Pin EIAJ Quad Flat Pack
  - 80 Pin Shrink Quad Flat Pack
- o Extended Temperature Range (-40C to +85C)
- o Direct replacement for Intel 80C186EB / 80C188EB / 80L186EB / 80L188EB microprocessors
- o Implemented with the Tekmos Customer Configured Microcontroller (CCM) technology.

General Description

The TK80C186EB and the TK80C188EB are all based on the same die. Unless otherwise noted, discussions of the TK80C186EB can be applied to both parts.

The TK80C186EB is an enhancement of the original 80C186EA microprocessor. It offers new features while remaining object code compatible with the original EA series of processors.

The TK80C186EB will work correctly at either 3 or 5 volts. The original Intel parts were sorted by minimum operating voltage to select the parts for the “L” series. With today’s improved process control, it is possible for all Tekmos parts to operate at both 3 and 5 volts. Orders for the “L” series will be filled with “C” parts.

The small feature sizes (0.35u) used in the TK80C186EB result in a significant power reduction as compared to the original devices. This is enhanced through use of the Idle and Powerdown modes. These modes stop portions of, or all of the internal clocks to achieve the power savings.

The TK80C186EB integrates commonly used system peripherals with the 186 CPU core to save space and reduce overall power consumption. A programmable interrupt controller supports and prioritizes 128 interrupts from internal, external, and software sources. The TK80C186EB also contains three programmable timer / counters and two serial channels.

Figure 1 shows the block diagram for the TK80C186EB / TK80C188EB.

Block Diagram

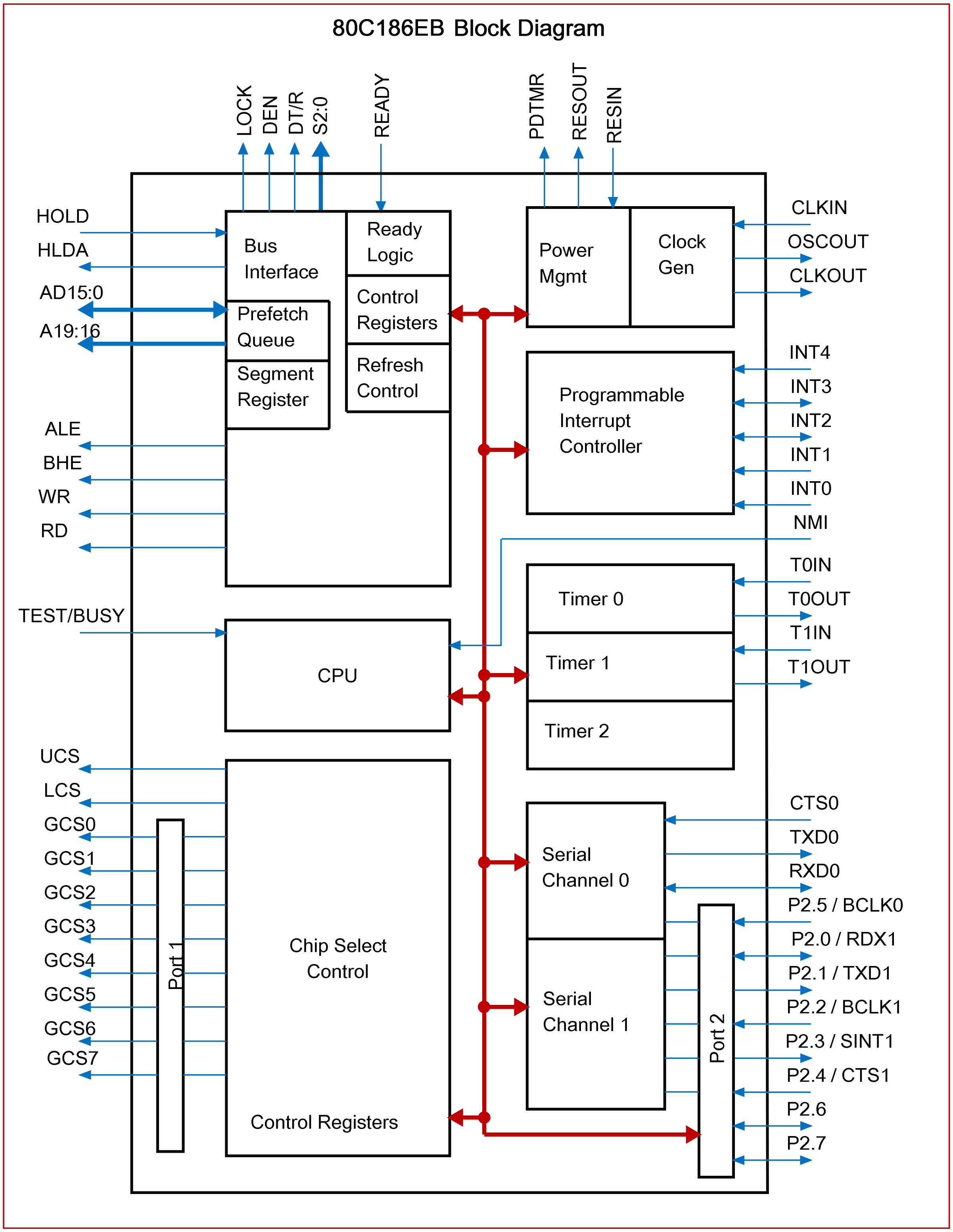

Figure 1, TK80C186EB / TK80C188EB Block Diagram

TK80C186EB Core Architecture

Bus Interface Unit

The bus interface unit generates the local bus control signals. It uses a HOLD / HLDA protocol to share the bus with other bus masters.

The Bus Interface Unit generates the 20 bit address, read strobe, write strobe, data, and bus cycle status information. It also reads data off of the local bus during a read operation. The READY pin optionally extends the bus cycle beyond the minimum 4 clocks.

The Bus Interface Unit also generates the DEN and DT/R control signals for external transceiver chips. This allows for the buffering of the multiplexed address / data bus.

Clock Generator

The TK80C186EB contains a clock generator that supports both internal and external clock generation. It consists of a crystal oscillator, a divide-by-two circuit, and clock gating circuitry to support the power-down and idle modes.

The clock generator can be used with either a crystal or it can be driven directly from an external clock source. Figure 2 shows the connections for both cases.

The crystal or clock frequency must be twice the desired operating frequency due to the divide-by-two circuit. This produces a 50% duty cycle on the internal clock, and makes the processor performance independent of duty cycle variations present on the input clock. The internal clock is available on the CLKOUT pin. All AC timings are referenced to the CLKOUT pin.

TK80C186EB Peripherals

The TK80C186EB contains a number of integrated peripherals. These flexible peripherals are integrated with each other to provide a solution to most processor applications.

The TK80C186EB contains the following peripherals:

- 7 / 10 Input Interrupt Controller
- 3 Channel Timer / Counter
- 2 Channel Serial Controller
- 10 Output Chip Select Controller
- DRAM Refresh Controller
- 2 8-bit parallel ports
- Power Management Logic

All of the peripheral control registers are contained within a 128x16 Peripheral Control Block (PCB). The PCB can be relocated to either memory or I/O space on any 256 byte address boundary.

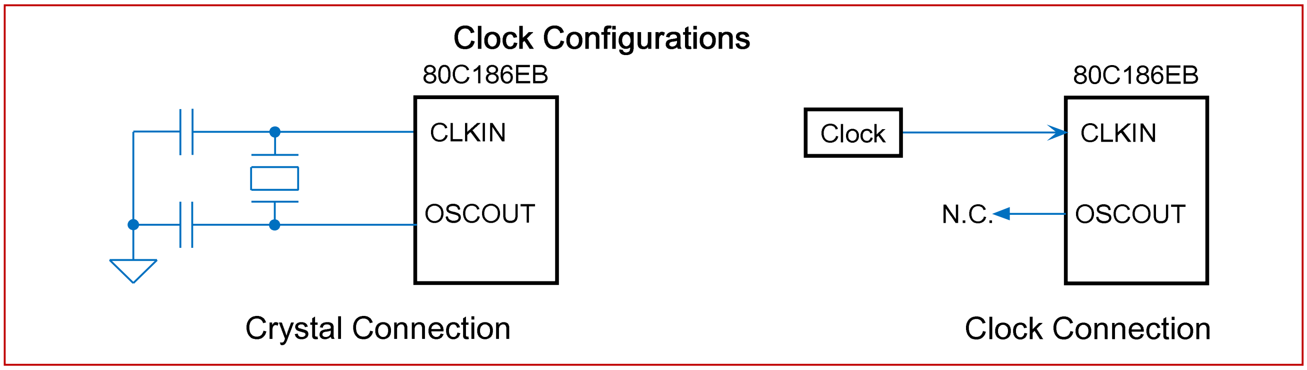

Figure 2 – Clock Configurations

Figure 3 shows the register assignments in the PCB.

Interrupt Controller

The interrupt controller receives both internal and external interrupt requests. It assigns a programmable priority to each interrupt before passing it on to the CPU. Each interrupt source can be individually enabled or disabled. There is also a global interrupt enable.

External interrupts come from the pins INT4:0, while internal interrupts come from the timers and serial channels. While there is only a single interrupt enable for all of the timers, each timer has its own interrupt vector. Serial Channel 0 also has a single interrupt enable with separate interrupt vectors for the transmit and receive interrupts. The interrupt for Serial Channel 1 is brought to an external pin, and may be connected to one of the external interrupts.

The NMI interrupt pin is directly connected to the CPU.

Serial Controller

The Serial controller contains two independent channels. Each channel has its own baud rate generator, or may be clocked through an external baud rate source.

Each serial channel has one synchronous mode and 4 asynchronous modes. These modes support various data lengths and parity options.

In addition, the serial channels support a multiprocessor protocol for devices connected to a common serial bus.

Timer / Counter

The timer / counter contains 3 16-bit timers. Two of them may be connected to external pins for clocking or control. The third timer is clocked internally, but may be used to provide a clock source to the other two timers.

The timers may be programmed to meet the needs of many applications, In addition to keeping track of the passage of time, they may also count or time external events, or generate non-repetitive waveforms.

Chip Select Controller

The Chip Select Controller generates up to 10 programmable chip selects for accessing both memories and peripherals. Each chip select can also be programmed to terminate a bus cycle independently of the state of the READY pin. The chip selects are available for all bus cycles, independent of the internal source (CPU or refresh).

Refresh Controller

The refresh controller supports the use of DRAMs by generating periodic read cycles of consecutive 12-bit addresses. The delay between the cycles is programmable up to 512 clocks. The high order address lines are also programmable to support refresh cycles on any 8K memory block.

Power Management

The power management logic provides two modes to control the power consumption. These are:

- Idle Mode
- Power Down Mode

The idle mode stops the CPU and Bus clocks, while allowing the peripheral clocks to continue to run. This reduces overall power while allowing the peripherals to remain active and to awaken the processor as necessary.

The power down mode stops the oscillator and all internal clocks. All registers maintain their values as long as Vdd is present. Current is reduced to leakage values.

PCB Register Assignments										
PCB	Function		PCB	Function		PCB	Function		PCB	Function
00	Reserved		40	Timer 2 Count		80	GCS0 Start		C0	Reserved
02	End of Interrupt		42	Timer 2 Compare		82	GCS0 Stop		C2	Reserved
04	Poll		44	Reserved		84	GCS1 Start		C4	Reserved
06	Poll status		46	Timer 2 Control		86	GCS1 Stop		C6	Reserved
08	Interrupt Mask		48	Reserved		88	GCS2 Start		C8	Reserved
0A	Priority Mask		4A	Reserved		8A	GCS2 Stop		CA	Reserved
0C	In-Service		4C	Reserved		8C	GCS3 Start		CC	Reserved
0E	Interrupt Req		4E	Reserved		8E	GCS3 Stop		CE	Reserved
10	Interrupt Status		50	Port 1 Direction		90	GCS4 Start		D0	Reserved
12	Timer Control		52	Port 1 Pin		92	GCS4 Stop		D2	Reserved
14	Serial Control		54	Port 1 Control		94	GCS5 Start		D4	Reserved
16	INT4 Control		56	Port 1 Latch		96	GCS5 Stop		D6	Reserved
18	INT0 Control		58	Port 2 Direction		98	GCS6 Start		D8	Reserved
1A	INT1 Control		5A	Port 2 Pin		9A	GCS6 Stop		DA	Reserved
1C	INT2 Control		5C	Port 2 Control		9C	GCS7 Start		DC	Reserved
1E	INT3 Control		5E	Port 2 Latch		9E	GCS7 Stop		DE	Reserved
20	Reserved		60	Serial 0 Baud		A0	LCS Start		E0	Reserved
22	Reserved		62	Serial 0 Count		A2	LCS Stop		E2	Reserved
24	Reserved		64	Serial 0 Control		A4	UCS Start		E4	Reserved
26	Reserved		66	Serial 0 Status		A6	UCS Stop		E6	Reserved
28	Reserved		68	Serial 0 RBUF		A8	Relocation		E8	Reserved
2A	Reserved		6A	Serial 0 TBUF		AA	Reserved		EA	Reserved
2C	Reserved		6C	Reserved		AC	Reserved		EC	Reserved
2E	Reserved		6E	Reserved		AE	Reserved		EE	Reserved
30	Timer 0 Count		70	Serial 1 Baud		B0	Refresh Base		F0	Reserved
32	Timer 0 Compare A		72	Serial 1 Count		B2	Refresh Time		F2	Reserved
34	Timer 0 Compare B		74	Serial 1 Control		B4	Refresh Control		F4	Reserved
36	Timer 0 Control		76	Serial 1 Status		B6	Reserved		F6	Reserved
38	Timer 1 Count		78	Serial 1 RBUF		B8	Power Control		F8	Reserved
3A	Timer 1 Compare A		7A	Serial 1 TBUF		BA	Reserved		FA	Reserved
3C	Timer 1 Compare B		7C	Reserved		BC	Step ID (=02h)		FC	Reserved
3E	Timer 1 Control		7E	Reserved		BE	Reserved		FE	Reserved

Figure 3 – PCB Register Assignments While in Master Mode

80C187 Interface (TK80C186EB Only)

The TK80C186EB does not support the interface to the external 80C187 math coprocessor. The interface pins are labeled for convenience.

Once Test Mode

The ONCE mode can be activated by forcing the A19 pin low during a processor reset. This in turn forces all input and output pins into a high-impedance state.

Pin Descriptions

VCC - Supply

Positive Power Supply

GND - Supply

Ground

CLKIN - Input

Clock Input. CLKIN is 2X the internal clock speed. CLKIN may be used with OSCOUT to create a crystal oscillator.

OSCOUT - Output

The OSCOUT pin is used with CLKIN to create a crystal oscillator. The OSCOUT pin should be left unconnected when CLKIN is directly driven.

CLKOUT - Output

CLKOUT is a divide-by-two of the CLKIN pin, triggering on every CLKIN falling edge. It is used as the timing references for all processor AC specifications.

RESIN* – Input

RESIN (Reset In) causes the processor to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the processor begins fetching opcodes at memory location 0FFFF0H.

RESOUT – Output

RESOUT (Reset Output) indicates the processor is currently in the reset state. RESOUT will remain active as long as RESIN remains active

PDTMR – Bidirectional

The PDTMR (Power-Down Timer) determines the amount of time the processor waits after an exit from power down before resuming normal operation. This pin is normally connected to an external capacitor. The duration of time required will depend on the startup characteristics of the crystal oscillator.

NMI – Input

The NMI (Non-Maskable Interrupt) pin causes a Type 2 interrupt to be serviced by the CPU. NMI is latched internally.

TEST* / BUSY – Input

The TEST* / BUSY pin is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (low). This pin also receives the BUSY signal from the 80C187 Numerics Coprocessor.

AD15 – AD0 – Bidirectional

These pins provide a multiplexed Address and Data bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle. In the -188 versions, pins AD8 to AD15 provide valid address information for the entire cycle.

A19 / ONCE* - A16 – Output

These pins provide multiplexed Address during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. These pins are driven to a logic 0 during the data phase of the bus cycle.

Forcing A19 low during reset triggers the ONCE mode.

S2, S1, S0 – Output

Bus cycle Status are encoded on these pins to provide bus transaction information. S2-S0 are encoded as follows:

S2	S1	S0	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Processor HALT
1	0	0	Queue Instruction Fetch
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive (no bus activity)

ALE – Output

Address Latch Enable output is used to latch address information during the address phase of the bus cycle.

BHE* – Output

Byte High Enable output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. BHE and A0 have the following logical encoding:

A0	BHE	Encoding (80C186EB Only)
0	0	Word Transfer
0	1	Even Byte Transfer
1	0	Odd Byte Transfer
1	1	Refresh Operation

On the 80C188EB/80L188EB, RFSH is asserted low to indicate a Refresh bus cycle.

RD* – Output

The RD* (Read) output signals that the accessed memory or I/O device must drive data information onto the data bus.

WR* – Output

The WR* (Write) output signals that data available on the data bus are to be written into the accessed memory or I/O device.

READY – Input

READY is an input to signal for the end of a bus cycle. READY must be active to terminate any processor bus cycle, unless it is ignored due to the programming of the Chip Select Unit.

DEN* – Output

The DEN* (Data Enable) output controls the enable of bidirectional transceivers in a buffered. DEN* is active only when data is to be transferred on the bus.

DT/R – Output

The DT* / R (Data Transmit/Receive) output controls the direction of a bidirectional buffer in a buffered system. DT/R is only available on the PLCC 84 package.

LOCK* – Output

LOCK* output indicates that the bus cycle in progress is not to be interrupted. The processor will not service other bus requests (such as HOLD) while LOCK* is active. This pin is configured as a weakly held high input while RESIN is active and must not be driven low.

HOLD – Input

HOLD request input to signal that an external bus master wishes to gain control of the local bus. The processor will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.

HLDA – Output

The HLDA (Hold Acknowledge) output indicates that the processor has relinquished control of the local bus. When HLDA is asserted, the processor has floated its data bus and control signals allowing another bus master to drive the signals directly.

NCS* – NC

The NCS* (Numeric Coprocessor Select) pin accesses the Numeric Coprocessor. This pin is not supported in the Tekmos design.

ERROR* – NC

The ERROR pin indicates that the last numeric coprocessor operation resulted in an exception condition. This pin is not supported in the Tekmos design.

PEREQ – NC

The PEREQ (Coprocessor Request) input signals that a data transfer between the external coprocessor and memory is pending. This pin is not supported in the Tekmos design.

UCS* – Output

Upper Chip Select will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, UCS* is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. During a processor reset, UCS* and LCS* are used to enable ONCE Mode.

LCS* – Output

Lower Chip Select will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. LCS is inactive after a reset.

P1.0 – P1.7 / GCS0* - GCS7*– Output

These pins provide a multiplexed function. If enabled, each pin can provide a generic chip select function. When not programmed as a chip select, each pin can function as a general purpose output port. As an output port, each pin can be read internally.

T0OUT, T1OUT – Output

The Timer Output pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.

T0IN, T1IN – Input

The Timer Inputs are used either as clock or control signals, depending on the timer mode selected.

INT0, INT1, INT4 – Input

Maskable Interrupt inputs will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with INTA0 and INTA1 to interface with an external slave controller.

INT2 / INTA0*, INT3 / INTA1* – Bidirectional

These pins provide multiplexed functions. As inputs, they provide a maskable interrupt that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an interrupt acknowledge handshake signal to allow interrupt expansion.

P2.7 / P2.6 – Bidirectional

These pins are bidirectional, open drain, general purpose port pins.

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CTS0*, P2.4 / CTS1* - Input

The Clear-To-Send function controls transmission on their respective serial channel.

TXD0, P2.1 / TXD1 – Output

These pins provide the Transmit Data for the serial channels. When operating in Mode 0, these pins provide the clock for the synchronous data on the RXD pins.

RXD0, P2.0 / RXD1 – Bidirectional

These pins are the receive data for the serial channels. In mode 0, these pins become bidirectional.

P2.5 / BCLK0, P2.2 / BCLK1 – Input

These bins provide an external baud clock for the serial channels.

P2.3 / SINT1 – Output

This is the serial interrupt for channel 1.

Reset Operation

Basic Operation

The reset pin is synchronized internally before it is applied to the rest of the circuit. This means that the clocks must be operating while RESIN* is low to insure correct initialization of the device.

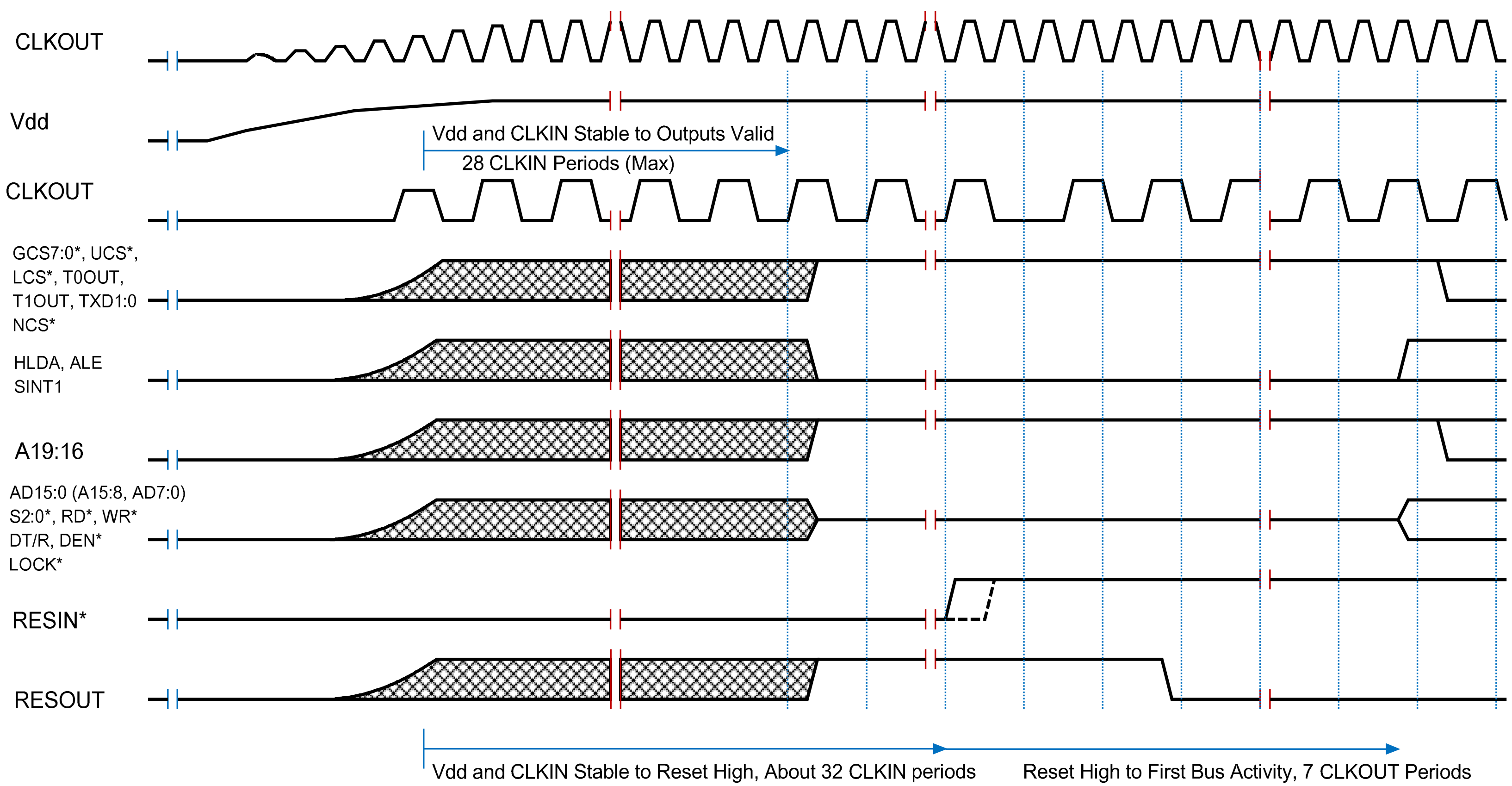
Cold Reset

It is important to insure that RESIN* remain active until the clocks have stabilized, If a RC reset circuit is used, the RC time constant must be longer than the power supply rise time.

Warm Reset

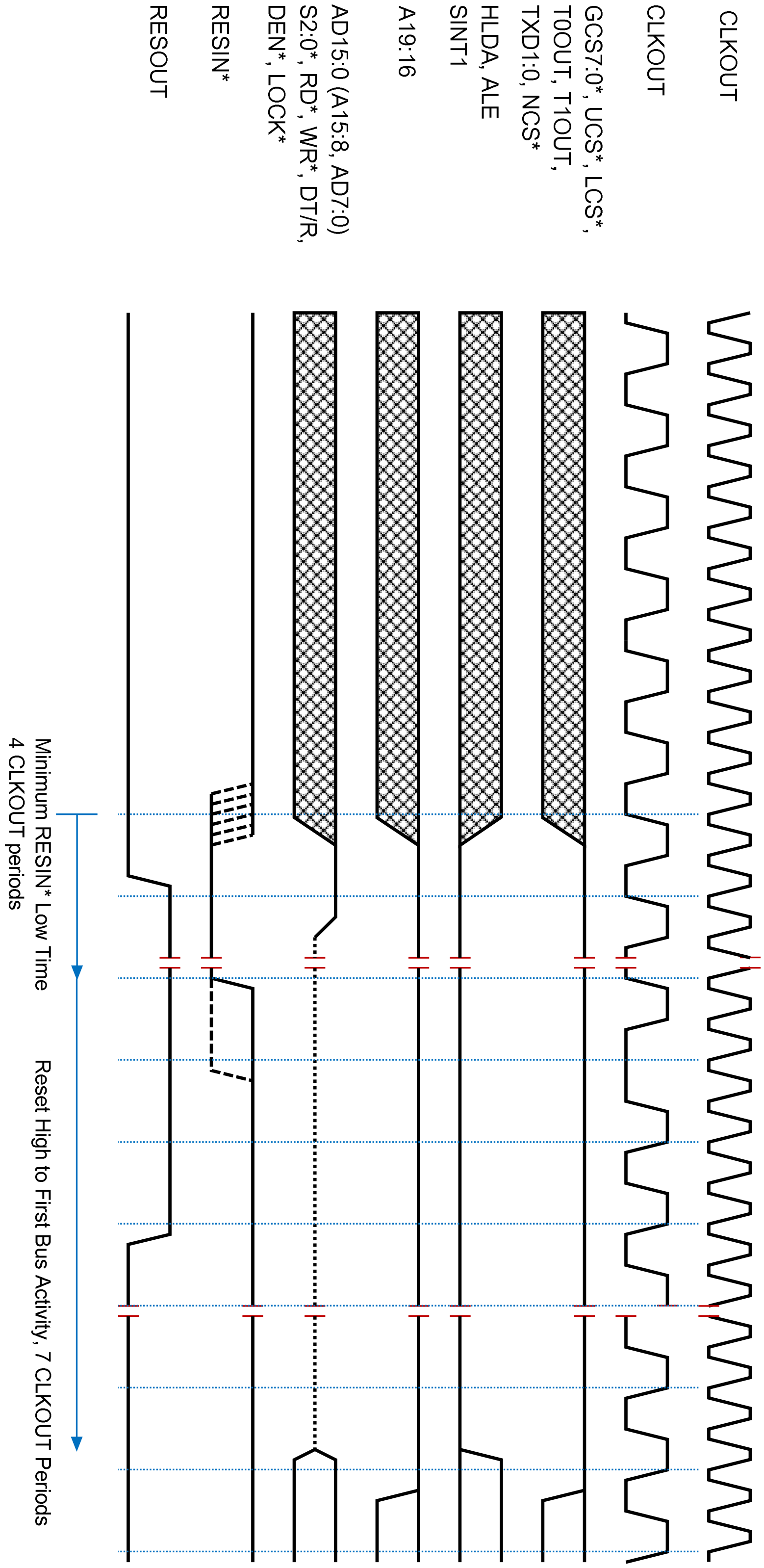
RESIN* must be remain low for four CLKOUT periods to take effect. A reset will terminate all activity and bus cycles.

Cold Reset Waveforms



Note:
CLKOUT synchronization occurs on the rising edge of RESIN*. If RESIN* is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If RESIN* is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.
Pin names in parentheses apply to 80C188EB.

Warm Reset Waveforms



Note:
CLKOUT synchronization occurs on the rising edge of RESIN*. If RESIN* is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If RESIN* is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.
Pin names in parentheses apply to 80C188EB.

Pinout

SQFP 80	PQFP 80	PLCC 84	80C186	80C 188
1	44	12	HLDA	
2	45	13	HOLD	
3	46	14	TEST* / BUSY	
4	47	15	LOCK*	
		16	DT/R*	
5	48	17	NMI	
6	49	18	READY	
7	50	19	P1.7 / GCS7*	
8	51	20	P1.6 / GCS6*	
9	52	21	P1.5 / GCS5*	
10	53	22	VSS	
11	54	23	VDD	
12	55	24	P1.4 / GCS4*	
13	56	25	P1.3 / GCS3*	
14	57	26	P1.2 / GCS2*	
15	58	27	P1.1 / GCS1*	
16	59	28	P1.0 / GCS0*	
17	60	29	LCS*	
18	61	30	UCS*	
19	62	31	INT0	
20	63	32	INT1	
21	64	33	INT2 / INTA0*	
22	65	34	INT3 / INTA1*	
23	66	35	INT4	
24	67	36	PDTMR	
25	68	37	RESIN*	
26	69	38	RESOUT	
		39	PEREQ	NC
27	70	40	OSCOUT	
28	71	41	CLKIN	
29	72	42	VDD	
30	73	43	VSS	
31	74	44	CLKOUT	
32	75	45	T0OUT	
33	76	46	T0IN	
34	77	47	T1OUT	
35	78	48	T1IN	
36	79	49	P2.7	
37	80	50	P2.6	
38	1	51	CTS0*	
39	2	52	TXD0	
40	3	53	RXD0	

SQFP 80	PQFP 80	PLCC 84	80C186	80C 188
41	4	54	P2.5 / BCLK0	
42	5	55	P2.3 / SINT1	
43	6	56	P2.4 / CTS1*	
44	7	57	P2.0 / RXD1	
45	8	58	P2.1 / TXD1	
46	9	59	P2.2 / BCLK1	
		60	NCS*	NC
47	10	61	AD0	
48	11	62	AD8	A8
49	12	63	VSS	
50	13	64	VDD	
51	14	65	VSS	
52	15	66	AD1	
53	16	67	AD9	A9
54	17	68	AD2	
55	18	69	AD10	A10
56	19	70	AD3	
57	20	71	AD11	A11
58	21	72	AD4	
59	22	73	AD12	A12
60	23	74	AD5	
61	24	75	AD13	A13
62	25	76	AD6	
63	26	77	AD14	A14
64	27	78	AD7	
65	28	79	AD15	A15
66	29	80	A16	
67	30	81	A17	
68	31	82	A18	
69	32	83	A19 / ONCE	
70	33	84	VSS	
71	34	1	VDD	
72	35	2	VSS	
		3	ERROR*	NC
73	36	4	RD*	
74	37	5	WR*	
75	38	6	ALE	
76	39	7	BHE*	RFSH*
77	40	8	S2*	
78	41	9	S1*	
79	42	10	S0*	
80	43	11	DEN*	

Electrical Specifications

Maximum Ratings

Characteristics		Symbol	Min	Max	Unit
Supply Voltage		Vdd	-0.5	5.5	V
Input Voltage		Vin	Vss – 0.3	Vdd + 0.3	V
Current Drain per Pin		I_{OL}		15	mA
Operating Temperature Range	Commercial Industrial	Tac Tai	0 -40	70 85	^oC ^oC
Storage Temperature range		Tstg	-55	+150	^oC

DC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = 0^oC to $+70^oC$)

Characteristics	Condition	Symbol	Min	Max	Unit
Supply Voltage		V_{DD}	4.5	5.5	V
Input Low Voltage		V_{IL}	-0.5	0.3 * Vdd	V
Input High Voltage		V_{IH}	0.7 * Vdd	5.5	V
Output Low Voltage	Iol = 3 mA	V_{OL}	0.0	0.45	V
Output High Voltage	Ioh = -2 mA	V_{OH}	Vdd - 0.5	Vdd	V
Input Hysteresis on /RESIN		V_{HYR}	0.50		V
Input Leakage Current for Pins: AD15:0, READY, HOLD, RESIN*, CLKIN, TEST*, NMI, INT4:0, T0IN, T1IN, RXD0, BCLK0, CTS0*, RXD1, BCLK1, CTS1*, SINT1, P2.6, P2.7	$0 < V_{IN} < V_{DD}$	I_{IL1}	-15	+15	uA
Input Leakage Current for Pins: A19/ONCE*, A18:A16, LOCK*	Note 1	I_{IL3}	-0.275	-5.0	mA
Output Leakage Current	$0.45 < V_{OUT} < V_{DD}$ Note 2	I_{OL}	-15	15	uA
Supply Current Cold (RESET) 25 MHz 20 MHz 13 MHz	 Note 3 Note 3 Note 3	I_{DD}		 115 108 73	 mA mA mA
Supply Current in Idle Mode 25 MHz 20 MHz 13 MHz	 Note 3 Note 3 Note 4	I_{ID}		 91 76 48	 mA mA mA
Supply Current in Powerdown Mode 25 MHz 20 MHz 13 MHz	 Note 3 Note 3 Note 3	I_{PD}		 100 100 100	 uA uA uA
Output Pin Capacitance	T_F = 1 MHz Note 4	C_{OUT}		15	pF
Input Pin Capacitance	T_F = 1 MHz	C_{IN}		15	pF

Notes:
1. RD/QSMD, /UCS, /LCS, /LOCK and /TEST/BUSY have an internal pullup that is activated during reset.
2. Output pins are floated during HOLD or ONCE mode.
3. Measured at worst case temperature and Vdd, and all outputs loaded.
4. Output capacitance is capacitive load of a floating output pin.

AC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Note	Symbol	Min	Max	Unit
Input Clock					
CLKIN Frequency	1	T_F	0	50	MHz
CLKIN Period	1	T_C	20		ns
CLKIN High Time	1, 2	T_{CH}	8		ns
CLKIN Low Time	1, 2	T_{CL}	8		ns
CLKIN Rise Time	1, 3	T_{CR}	1	7	ns
CLKIN Fall Time	1, 3	T_{CF}	1	7	ns
Output Clock					
CLKIN to CLKOUT Delay	1, 4	T_{CD}	0	16	ns
CLKOUT Period	1	T		$2T_C$	ns
CLKOUT High Time	1	T_{PH}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Low Time	1	T_{PL}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Rise Time	1, 5	T_{PR}	1	6	ns
CLKOUT Fall Time	1, 5	T_{PF}	1	6	ns
Output Delays					
ALE, S2:0*, DEN*, DT/R, BHE, RFSH, LOCK, A19:16	1, 4, 6, 7	T_{CHOV1}	3	17	ns
GCS7:0*, LCS*, UCS*, RD*, WR*	1, 4, 6, 8	T_{CHOV2}	3	20	ns
BHE*, RFSH*, DEN*, LOCK*, RESOUT, HLDA, T0OUT, T1OUT, A19:16	1, 4, 6	T_{CLOV1}	3	17	ns
RD*, WR*, GCS7:0*, LCS*, UCS*, AD15:0, INTA1:0*, S2:0*	1, 4, 6	T_{CLOV2}	3	20	ns
RD*, WR*, BHE*, RFSH*, DT/R*, LOCK*, S2:0*, A19:16	1	T_{CHOF}	0	20	ns
DEN*, AD15:0	1	T_{CLOF}	0	20	ns
Synchronous Inputs					
TEST, NMI, INT3:0, T1:0IN, ARDY	1, 7	T_{CHIS}	8		ns
TEST, NMI, INT3:0, T1:0IN, ARDY	1, 7	T_{CHIH}	3		ns
AD15:0, ARDY, SRDY, DRQ1:0	1, 7	T_{CLIS}	10		ns
AD15:0, ARDY, SRDY, DRQ1:0	1, 7	T_{CLIH}	3		ns
HOLD	1, 7	T_{CLIS}	10		ns
HOLD	1, 7	T_{CLIH}	3		ns
RESIN (to CLKIN)	1, 7	T_{CLIS}	10		ns
RESIN (From CLKIN)	1, 7	T_{CLIH}	3		ns

Notes:
1. See AC Waveforms for waveforms and definition
2. Measured at VIH for high time, VIL for low time.
3. Only required to guarantee IDD, Maximum limits are bounded by TC, TCH and TCL.
4. Specified for 50 pF load.
5. TCHOV1 applies to BHE, RFSH LOCK and A19:16 only after a HOLD release
6. TCHOV2 applies to RD and WR only after a HOLD release.
7. Setup and Hold are required to guarantee recognition
8. TCHOVS applies to BHE, RFSH and A19:16 only after a HOLD release.
9. AC measurements made with a 50 pF load, at a 50% supply voltage level.
10. Float delay measured with a 3.3K resistor tied to opposite supply, measured after a +/- 0.2V change in voltage level.

DC Electrical Specifications (Vdd = 3.3 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Condition	Symbol	Min	Max	Unit
Supply Voltage		V_{DD}	3.0	5.5	V
Input Low Voltage		V_{IL}	-0.5	0.3 * Vdd	V
Input High Voltage		V_{IH}	0.7 * Vdd	Vdd + 0.5	V
Output Low Voltage	Iol = 1.6 mA Note 1	V_{OL}	0.0	0.45	V
Output High Voltage	Ioh = -1 mA Note 1	V_{OH}	Vdd - 0.5	Vdd	V
Input Hysteresis on /RESIN		V_{HYR}	0.50		V
Input Leakage Current for Pins: AD15:0, READY, HOLD, RESIN*, CLKIN, TEST*, NMI, INT4:0, T0IN, T1IN, RXD0, BCLK0, CTS0*, RXD1, BCLK1, CTS1*, SINT1, P2.6, P2.7	$0 < V_{IN} < V_{DD}$	I_{IL1}	-15	+15	uA
Input Leakage Current for Pins: A19/ONCE*, A18:A16, LOCK*	Note 2	I_{IL3}	-0.275	-2.0	mA
Output Leakage Current	$0.45 < V_{OUT} < V_{DD}$ Note 3	I_{OL}	-15	15	uA
Supply Current Cold (RESET, 3.3V) 16 MHz	Note 4	I_{DD}		54	mA
Supply Current in Idle Mode (3.3V) 16 MHz	Note 5	I_{ID}		38	mA
Supply Current in Powerdown (3.3V) 16 MHz	Note 6	I_{PD}		140	uA
Output Pin Capacitance	T_F = 1 MHz Note 7	C_{OUT}		15	pF
Input Pin Capacitance	T_F = 1 MHz	C_{IN}		15	pF

Notes:

1. Ioh and Iol measured at Vdd = 3.0V
2. RD/QSMD, /UCS, /LCS, /LOCK and /TEST/BUSY have an internal pullup that is activated during reset.
3. Output pins are floated during HOLD or ONCE mode.
4. Measured during RESET, with worst case frequency, Vdd, and temperature, and with all outputs loaded as specified under AC Test Conditions, and all floating outputs driven to a supply.
5. Measured during HALT and IDLE mode active, with worst case frequency, Vdd, and temperature, and with all outputs loaded as specified under AC Test Conditions, and all floating outputs driven to a supply.
6. Measured during HALT and Powerdown mode active, with worst case frequency, Vdd, and temperature, and with all outputs loaded as specified under AC Test Conditions, and all floating outputs driven to a supply.
7. Output capacitance is capacitive load of a floating output pin.

AC Electrical Specifications (Vdd = 3.3 V +/- 10%, Vss = 0 V, Ta = 0^oC to $+70^oC$)

Characteristics	Note	Symbol	Min	Max	Unit
Input Clock					
CLKIN Frequency	1	T_F	0	32	MHz
CLKIN Period	1	T_C	31.25		ns
CLKIN High Time	1, 2	T_{CH}	13		ns
CLKIN Low Time	1, 2	T_{CL}	13		ns
CLKIN Rise Time	1, 3	T_{CR}	1	8	ns
CLKIN Fall Time	1, 3	T_{CF}	1	8	ns
Output Clock					
CLKIN to CLKOUT Delay	1, 4	T_{CD}	0	30	ns
CLKOUT Period	1	T		$2T_C$	ns
CLKOUT High Time	1	T_{PH}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Low Time	1	T_{PL}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Rise Time	1, 5	T_{PR}	1	9	ns
CLKOUT Fall Time	1, 5	T_{PF}	1	9	ns
Output Delays					
DT/R, RFSH, LOCK, A19:16	1, 4, 6, 7	T_{CHOV1}	3	22	ns
GCS7:0*, LCS*, UCS*, RD*, WR*	1, 4, 6, 8	T_{CHOV2}	3	27	ns
BHE*, DEN*	1, 4	T_{CHOV3}	3	25	ns
ALE	1, 4	T_{CHOV4}	3	30	ns
S2:0*	1, 4	T_{CHOV5}	3	33	ns
LOCK*, RESOUT, HLDA, T0OUT, T1OUT, A19:16	1, 4, 6	T_{CLOV1}	3	25	ns
RD*, WR*, GCS7:0*, LCS*, UCS*, AD15:0, INTA1:0*,	1, 4, 6	T_{CLOV2}	3	30	ns
BHE*, DEN*, RFSH*,	1, 4, 6	T_{CLOV3}	3	25	ns
S2:0*	1, 4, 6	T_{CLOV5}	3	33	ns
RD*, WR*, BHE*, RFSH*, DT/R*, LOCK*, S2:0*, A19:16	1	T_{CHOF}	0	30	ns
DEN*, AD15:0	1	T_{CLOF}	0	30	ns
Synchronous Inputs					
TEST, NMI, INT3:0, T1:0IN, ARDY	1, 7	T_{CHIS}	15		ns
TEST, NMI, INT3:0, T1:0IN, ARDY	1, 7	T_{CHIH}	3		ns
AD15:0, ARDY, SRDY, DRQ1:0	1, 7	T_{CLIS}	15		ns
AD15:0, ARDY, SRDY, DRQ1:0	1, 7	T_{CLIH}	3		ns
HOLD	1, 7	T_{CLIS}	15		ns
HOLD	1, 7	T_{CLIH}	3		ns
RESIN (to CLKIN)	1, 7	T_{CLIS}	15		ns
RESIN (From CLKIN)	1, 7	T_{CLIH}	3		ns

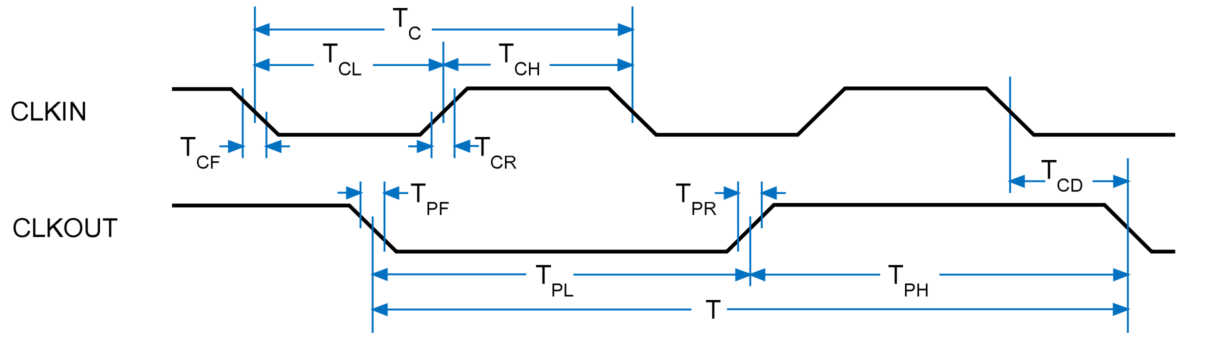
Notes:
1. See AC Waveforms for waveforms and definition
2. Measured at VIH for high time, VIL for low time.
3. Only required to guarantee IDD, Maximum limits are bounded by TC, TCH and TCL.
4. Specified for 50 pF load.
5. Specified for 50 pF load.
6. See Rise and Fall time waveform.
7. TCHOV1 applies to BHE, RFSH LOCK and A19:16 only after a HOLD release
8. TCHOV2 applies to RD and WR only after a HOLD release.
9. Setup and Hold are required to guarantee recognition
10. Setup and Hold are required for proper operation

AC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

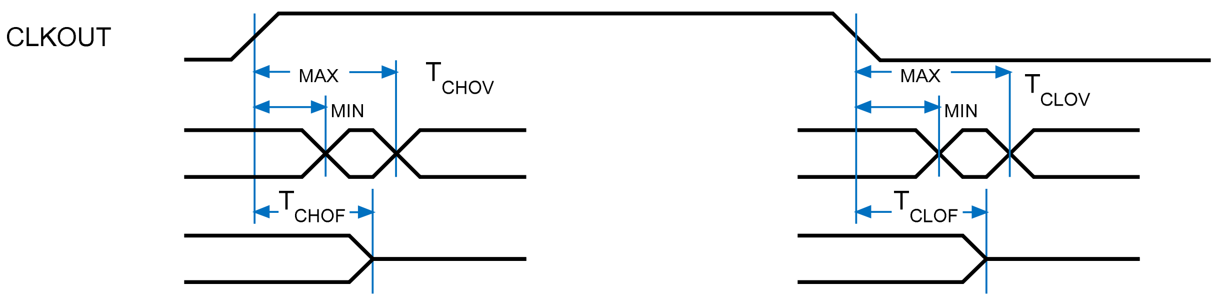
Characteristics	Note	Symbol	Min	Max	Unit
Relative Timings					
ALE Rising to ALE Falling		T_{LHLL}	T - 15		ns
Address Valid to ALE Falling		T_{AVLL}	(T/2) - 10		ns
Chip Selects Valid to ALE Falling	1	T_{PLLL}	(T/2) - 10		ns
Address Hold form ALE Falling		T_{LLAX}	(T/2) - 10		ns
ALE Falling to WR* Falling	1	T_{LLWL}	(T/2) - 15		ns
ALE Falling to RD* Falling	1	T_{LLRL}	(T/2) - 15		ns
WR* Rising to ALE Rising	1	T_{WHLH}	(T/2) - 10		ns
Address Float to RD* Falling		T_{AFRL}	0		ns
RD* Falling to RD* Rising	2	T_{RLRH}	(2*T) - 5		ns
WR* Falling to WR* Rising	2	T_{WLWH}	(2*T) - 5		ns
RD* Rising to Address Active		T_{RHAV}	T - 15		ns
Output Data Hold after WR Rising		T_{WHDX}	T - 15		ns
WR* Rising to Chip Select Rising	1	T_{WHPH}	3(T/2) - 10		ns
RD* Rising to Chip Select Rising	1	T_{RHPH}	(T/2) - 10		ns
CS* Inactive to CS* Active	1	T_{PHPL}	(T/2) - 10		ns
ONCE* Active to RESIN* Rising	3	T_{OVRH}	T		ns
ONCE* Hold from RESIN* Rising	3	T_{RHOX}	T		ns

Notes:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested

Clock Waveforms

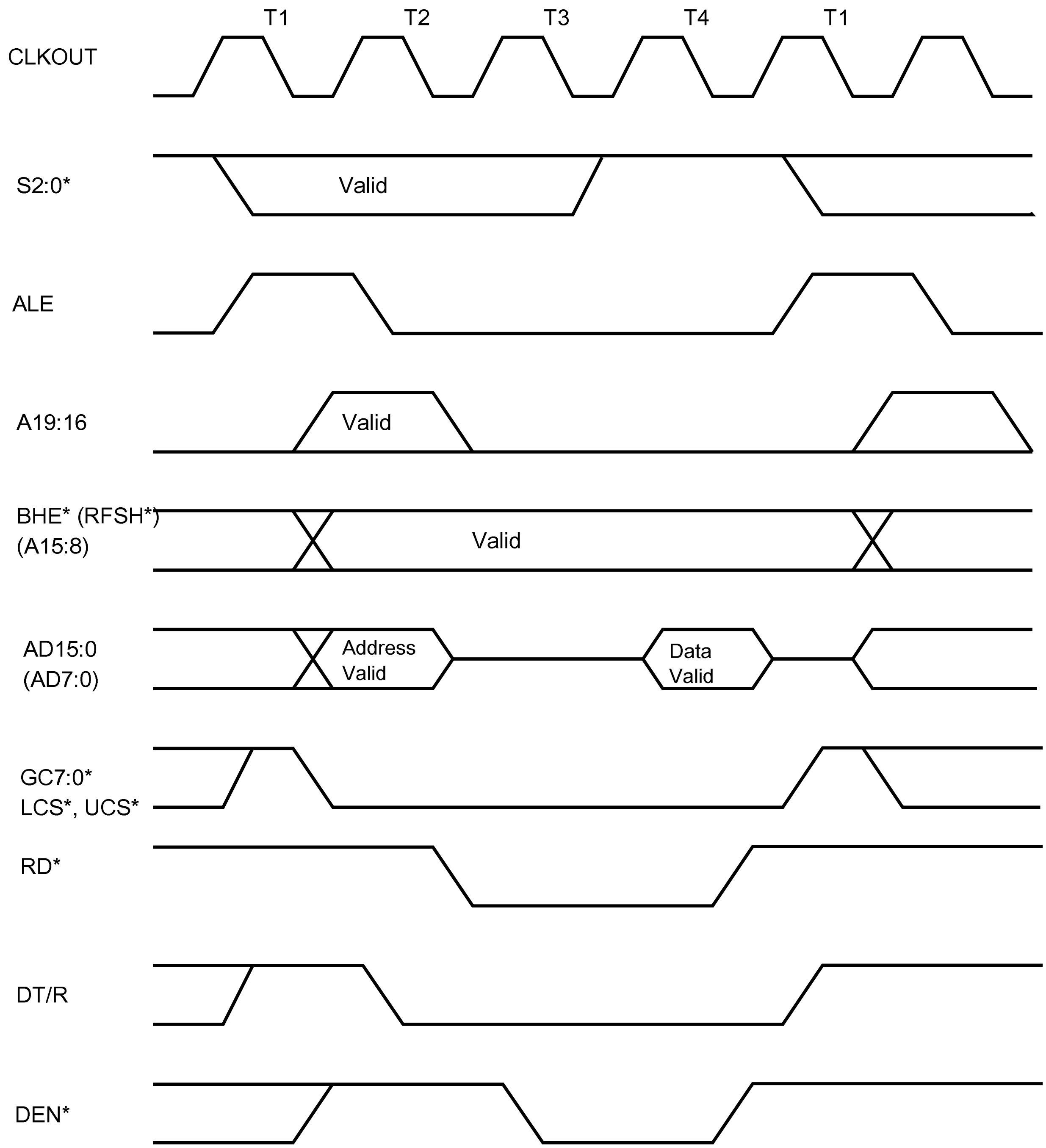


Output Delay and Float Waveforms

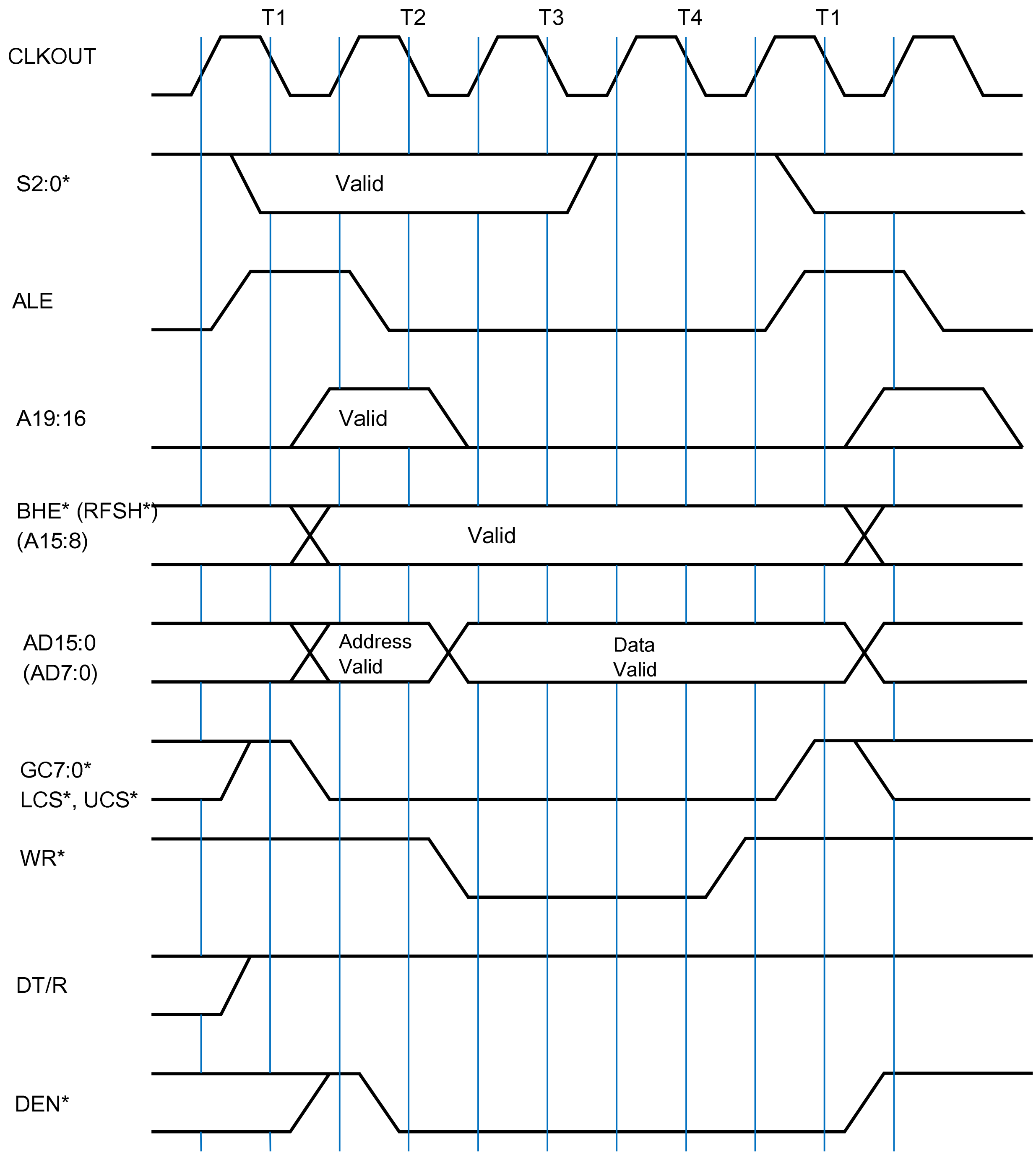


Input Setup and Hold Waveforms

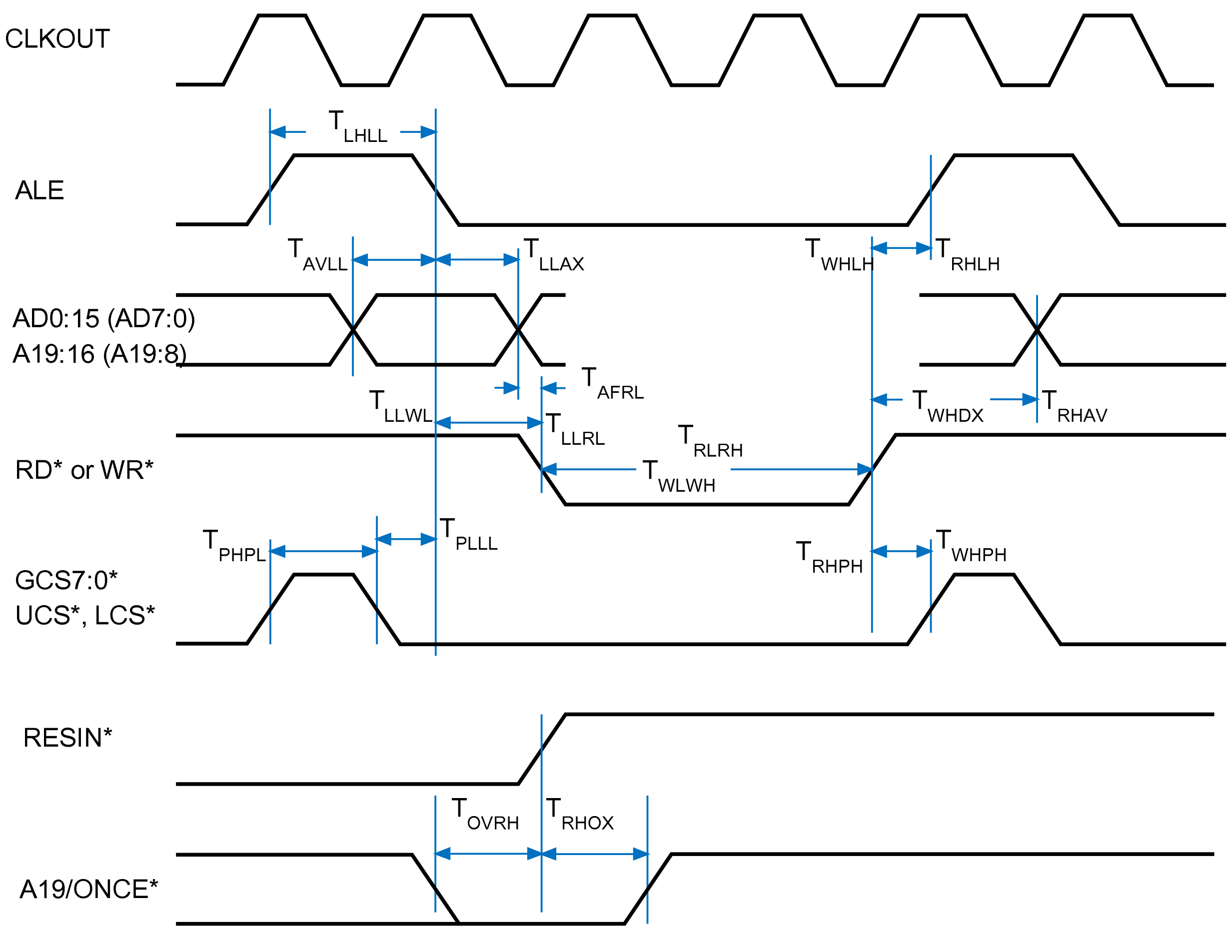
Read, Fetch, and Refresh Cycle Waveforms



Write Cycle Waveforms



Relative Signal Waveforms



Errata

1. The RESIN* pin uses a standard CMOS input. It is supposed to have a Schmitt trigger.

2. The ability to read the status of an external level sensitive interrupt is blocked by the mask bits. This can affect some polled interrupt applications.

3. The chip select signals are unnecessarily extended beyond the write strobes.

All errata will be corrected in the next revision.

Ordering Information

Code	Temperature	Package	Frequency	Replaces
TK80C186EB-25CA	0 to +70	Plastic 84 PLCC – RoHS	25 MHz	N80C186EB25
TK80C186EB-25CB	0 to +70	Plastic 80 PQFP – RoHS	25 MHz	S80C186EB25
TK80C186EB-25CT	0 to +70	Plastic 80 TQFP – RoHS	25 MHz	SB80C186EB25
TK80C186EB-25IA	-40 to +85	Plastic 84 PLCC – RoHS	25 MHz	TN80C186EB25
TK80C186EB-25IB	-40 to +85	Plastic 80 PQFP – RoHS	25 MHz	TS80C186EB25
TK80C186EB-25IT	-40 to +85	Plastic 80 TQFP – RoHS	25 MHz	TSB80C186EB25
TK80C188EB-25CA	0 to +70	Plastic 84 PLCC – RoHS	25 MHz	N80C188EB25
TK80C188EB-25CB	0 to +70	Plastic 80 PQFP – RoHS	25 MHz	S80C188EB25
TK80C188EB-25CT	0 to +70	Plastic 80 TQFP – RoHS	25 MHz	SB80C188EB25
TK80C188EB-25IA	-40 to +85	Plastic 84 PLCC – RoHS	25 MHz	TN80C188EB25
TK80C188EB-25IB	-40 to +85	Plastic 80 PQFP – RoHS	25 MHz	TS80C188EB25
TK80C188EB-25IT	-40 to +85	Plastic 80 TQFP – RoHS	25 MHz	TSB80C188EB25
TK80C188EB-25ITR	-40 to +85	Plastic 80 TQFP – Non-RoHS	25 MHz	Step ID = 5

Contact Information

The TK80C186 series may be ordered directly from Tekmos

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Revision History

Date	Revision	Description
2/09/09	1.0	Initial release
9/28/09	1.1	Fix error in interrupt description
10/01/09	1.2	Add Non-RoHS version with Step ID = 5
4/05/10	1.3	Add errata, 3.3v specifications, expand timing diagrams, reset