

Features

- Static 186 CPU core.
- Clock Generator
- 3 Programmable 16-Bit Timers
- 2 DMA Channels
- Programmable Memory and Peripheral Chip Selects
- Memory Refresh Generator
- High Impedance Test Mode (ONCE)
- High Speed Operation (25 MHz)
- 1 MB Memory Address Capability
- 64 KB I/O Address Capability
- Available in the Following Packages:
 - 68 Pin PLCC
 - 80 Pin EIAJ Quad Flat Pack
 - 80 Pin Shrink Quad Flat Pack
- Extended Temperature Range (-40C to +85C)
- Direct replacement for Intel 80C186XL / 80C188XL microprocessors
- Implemented with the Tekmos Customer Configured Microcontroller (CCM) technology.

General Description

The TK80C186XL and the TK80C188XL are both all based on the same die. Unless otherwise noted, discussions of the TK80C186XL can be applied to both parts.

The TK80C186XL is an enhancement of the original 80C86 microprocessor. It offers new features while remaining object code compatible with the original processors.

The small feature sizes (0.35u) used in the TK80C186XL result in a significant power reduction as compared to the original devices. This is enhanced through use of the Power-Save mode, which adjusts the internal clock speed to achieve the power savings.

The TK80C186XL integrates commonly used system peripherals with the 186 CPU core to save space and reduce overall power consumption. A programmable interrupt controller supports and prioritizes 128 external interrupts in addition to the internal interrupts. The TK80C186XL also contains three programmable timer / counters and two DMA channels.

Figure 1 shows the block diagram for the TK80C186XL / TK80C188XL.

This is a preliminary product specification. Actual numbers and features may change when the actual product is released. Interested customers are welcome to evaluate the design as implemented in a FPGA based daughtercard.

Block Diagram

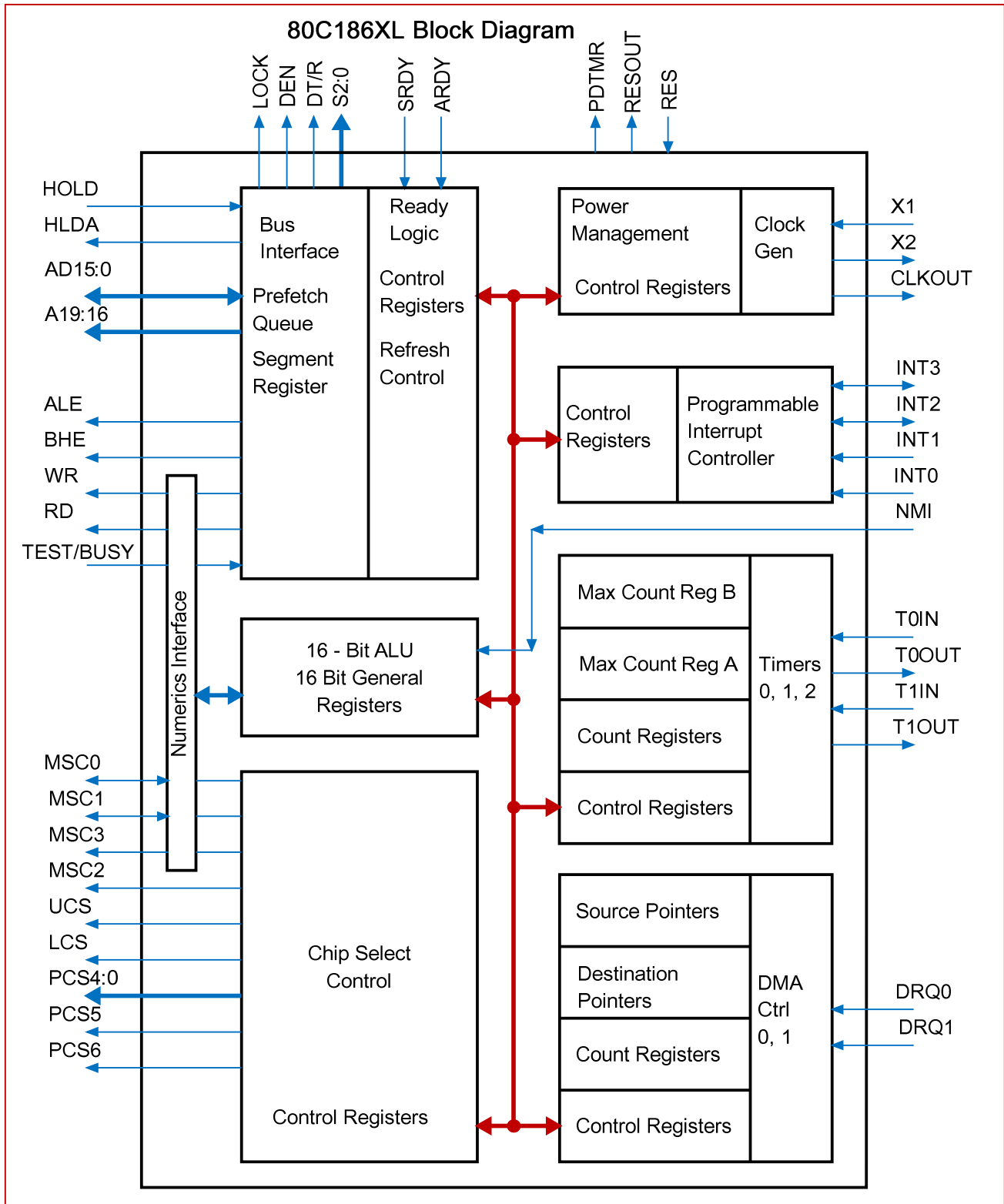


Figure 1, TK80C186XL / TK80C188XL Block Diagram

TK80C186XL Core Architecture

Bus Interface Unit

The bus interface unit generates the local bus control signals. It uses a HOLD / HLDA protocol to share the bus with other bus masters.

The Bus Interface Unit generates the 20 bit address, read strobe, write strobe, data, and bus cycle status information. It also reads data off of the local bus during a read operation. The READY pin optionally extends the bus cycle beyond the minimum 4 clocks.

The Bus Interface Unit also generates the DEN and DT/R control signals for external transceiver chips. This allows for the buffering of the multiplexed address / data bus.

Clock Generator

The TK80C186XL contains a clock generator that supports both internal and external clock generation. It consists of a crystal oscillator, a divide-by-two circuit, and clock gating circuitry to support the power-save mode.

The clock generator can be used with either a crystal or it can be driven directly from an external clock source. Figure 2 shows the connections for both cases.

The crystal or clock frequency must be twice the desired operating frequency due to the divide-by-two circuit. This produces a 50% duty cycle on the internal clock, and makes the processor performance independent of duty cycle variations present on the input clock. The internal clock is available on the CLKOUT pin. All AC timings are referenced to the CLKOUT pin.

TK80C186XL Peripherals

The TK80C186XL contains a number of integrated peripherals. These flexible peripherals are integrated with each other to provide a solution to most processor applications.

The TK80C186XL contains the following peripherals:

- 7 / 10 Input Interrupt Controller
- 3 Channel Timer / Counter
- 2 Channel DMA Controller
- 10 Output Chip Select Controller
- DRAM Refresh Controller
- 2 8-bit parallel ports
- Power Management Logic

All of the peripheral control registers are contained within a 128x16 Peripheral Control Block (PCB). The PCB can be relocated to either memory or I/O space on any 256 byte address boundary.

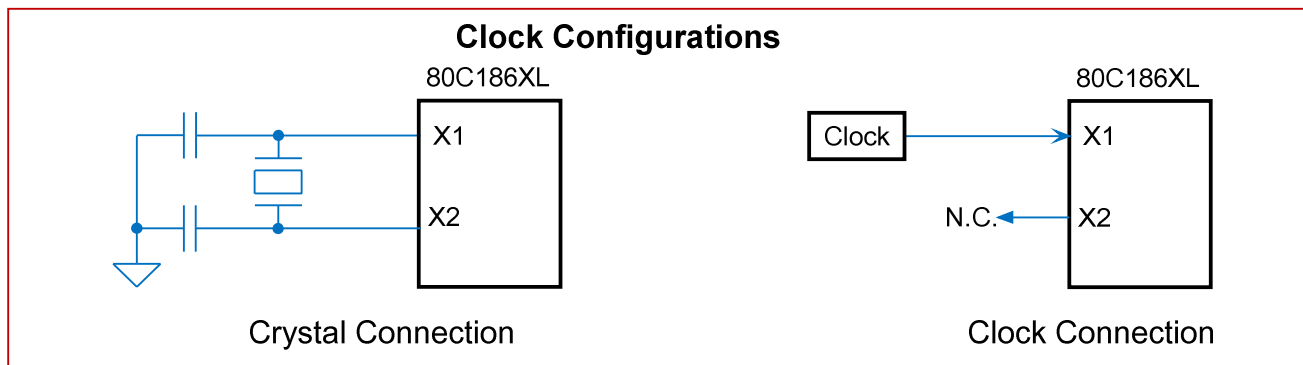


Figure 2 – Clock Configurations

Figure 3 shows the register assignments in the PCB.

Interrupt Controller

The interrupt controller receives both internal and external interrupt requests. It assigns a programmable priority to each interrupt before passing it on to the CPU. Each interrupt source can be individually enabled or disabled. There is also a global interrupt enable.

External interrupts come from the pins INT3:0, while internal interrupts come from the timers and DMA channels. While there is only a single interrupt enable for all of the timers, each timer has its own interrupt vector. Each DMA channel has its own interrupt vector.

The NMI interrupt pin is directly connected to the CPU.

DMA Controller

The DMA controller contains two independent channels. Data transfers can occur between memory and I/O, memory to memory, and I/O to I/O. Data can be transferred in bytes or words, and from or to even or odd addresses.

Each DMA channel maintains a 20 bit source and destination pointers. Each pointer may be optionally incremented or decremented after each transfer.

Each DMA cycle requires two bus cycles, which is a minimum of 8 clocks.

Timer / Counter

The timer / counter contains 3 16-bit timers. Two of them may be connected to external pins for clocking or control. The third timer is clocked internally, but may be used to provide a clock source to the other two timers.

The timers may be programmed to meet the needs of many applications. In addition to keeping track of the passage of time, they may also count or time

external events, or generate non-repetitive waveforms.

Chip Select Controller

The Chip Select Controller generates up to 10 programmable chip selects for accessing both memories and peripherals. Each chip select can also be programmed to terminate a bus cycle independently of the state of the READY pin. The chip selects are available for all bus cycles, independent of the internal source (CPU or refresh).

Refresh Controller

The refresh controller supports the use of DRAMs by generating periodic read cycles of consecutive 12-bit addresses. The delay between the cycles is programmable up to 512 clocks. The high order address lines are also programmable to support refresh cycles on any 8K memory block.

Power Save Mode

The power save mode logic provides the ability to reduce the clock speed for the internal logic. This is a direct savings in power consumption. The clock speed can be switched at any time under software control,

80C187 Interface (TK80C186XL Only)

The TK80C186XL does not support the interface to the external 80C187 math coprocessor. The interface pins are labeled for convenience.

Once Test Mode

The ONCE mode can be activated by forcing the UCS* and LCS* pins low while keeping RES* low. Bringing RES* back high latches in the ONCE mode.

Queue-Status Mode

The Queue Status mode is entered by holding RD low during the release of reset. Once entered, the ALE and WR pins become QS0 and QS1, respectively.

PCB Register Assignments							
PCB	Function	PCB	Function	PCB	Function	PCB	Function
00	Reserved	40	Reserved	80	Reserved	C0	D0SRCL
02	Reserved	42	Reserved	82	Reserved	C2	D0SRCH
04	Reserved	44	Reserved	84	Reserved	C4	D0DSTL
06	Reserved	46	Reserved	86	Reserved	C6	D0DSTH
08	Reserved	48	Reserved	88	Reserved	C8	D0TC
0A	Reserved	4A	Reserved	8A	Reserved	CA	D0CON
0C	Reserved	4C	Reserved	8C	Reserved	CC	Reserved
0E	Reserved	4E	Reserved	8E	Reserved	CE	Reserved
10	Reserved	50	T0CNT	90	Reserved	D0	D1SRCL
12	Reserved	52	T0CMPA	92	Reserved	D2	D1SRCH
14	Reserved	54	T0CMPB	94	Reserved	D4	D1DSTL
16	Reserved	56	T0CON	96	Reserved	D6	D1DSTH
18	Reserved	58	T1CNT	98	Reserved	D8	D1TC
1A	Reserved	5A	T1CMPA	9A	Reserved	DA	D1CON
1C	Reserved	5C	T1CMPB	9C	Reserved	DC	Reserved
1E	Reserved	5E	T1CON	9E	Reserved	DE	Reserved
20	Reserved	60	T2CNT	A0	UMCS	E0	RFBASE
22	EOI	62	T2CMPA	A2	LMCS	E2	RFTIME
24	POLL	64	Reserved	A4	PACS	E4	RFCON
26	POLLSTS	66	T2CON	A6	MMCS	E6	Reserved
28	IMASK	68	Reserved	A8	MPCS	E8	Reserved
2A	PRIMSK	6A	Reserved	AA	Reserved	EA	Reserved
2C	INSERV	6C	Reserved	AC	Reserved	EC	Reserved
2E	REQST	6E	Reserved	AE	Reserved	EE	Reserved
30	INSTS	70	Reserved	B0	Reserved	F0	PWRSVAV
32	TCUCON	72	Reserved	B2	Reserved	F2	PWRCON
34	DMA0CON	74	Reserved	B4	Reserved	F4	Reserved
36	DMA1CON	76	Reserved	B6	Reserved	F6	Step ID
38	I0CON	78	Reserved	B8	Reserved	F8	Reserved
3A	I1CON	7A	Reserved	BA	Reserved	FA	Reserved
3C	I2CON	7C	Reserved	BC	Reserved	FC	Reserved
3E	I3CON	7E	Reserved	BE	Reserved	FE	Relocation

Figure 3 – PCB Register Assignments While in Master Mode

Pin Descriptions

VDD - Supply

Positive Power Supply

VSS - Supply

Ground

X1 - Input

Clock Input. X1 is 2X the internal clock speed. X1 may be used with X2 to create a crystal oscillator.

X2 - Output

The OSCOUT pin is used with X1 to create a crystal oscillator. The X2 pin should be left unconnected when X1 is directly driven.

CLKOUT - Output

CLKOUT is a divide-by-two of the X1 pin, triggering on every X1 falling edge. It is used as the timing references for all processor AC specifications.

RES* - Input

RES* (Reset In) causes the processor to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESET will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with X1 before the processor begins fetching opcodes at memory location 0FFFF0H.

RESET - Output

RESOUT (Reset Output) indicates the processor is currently in the reset state. RESOUT will remain active as long as RESIN remains active

NMI - Input

The NMI (Non-Maskable Interrupt) pin causes a Type 2 interrupt to be serviced by the CPU. NMI is latched internally.

TEST* / BUSY - Input

The TEST* / BUSY pin is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (low). This pin also

receives the BUSY signal from the 80C187 Numerics Coprocessor.

AD15 – AD0 – Bidirectional

These pins provide a multiplexed Address and Data bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle. In the -188 versions, pins AD8 to AD15 provide valid address information for the entire cycle.

A19 - A16 – Output

These pins provide multiplexed Address during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. These pins are driven to a logic 0 during the data phase of the bus cycle.

These pins also contain the bus cycle status bits S3 – S6.

S2, S1, S0 – Output

Bus cycle Status are encoded on these pins to provide bus transaction information. S2-S0 are encoded as follows:

S2	S1	S0	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Processor HALT
1	0	0	Queue Instruction Fetch
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive (no bus activity)

ALE – Output

Address Latch Enable output is used to latch address information during the address phase of the bus cycle.

This pin also provides the QS0 – Queue Status Bit 0.

BHE* – Output

Byte High Enable output to indicate that the bus cycle in progress is transferring data over the upper

half of the data bus. BHE and A0 have the following logical encoding:

A0	BHE	Encoding (80C186XL Only)
0	0	Word Transfer
0	1	Even Byte Transfer
1	0	Odd Byte Transfer
1	1	Refresh Operation

On the 80C188XL/80L188XL, RFSH is asserted low to indicate a Refresh bus cycle.

RD* – Output

The RD* (Read) output signals that the accessed memory or I/O device must drive data information onto the data bus.

This pin also provides the QSMD* signal. Pulling this pin low during reset enables the Queue Status Mode.

WR* – Output

The WR* (Write) output signals that data available on the data bus are to be written into the accessed memory or I/O device.

This pin also provides the QS1 – Queue Status Bit 1 – signal during the Queue Status Mode.

ARDY – Input

Asynchronous ready is an input to signal for the end of a bus cycle. ARDY must be active to terminate a processor bus cycle.

SRDY – Input

Synchronous Ready is an input to signal for the end of a bus cycle. SRDY must be active to terminate a processor bus cycle.

DEN* – Output

The DEN* (Data Enable) output controls the enable of bidirectional transceivers in a buffered. DEN* is active only when data is to be transferred on the bus.

DT/R – Output

The DT* / R (Data Transmit/Receive) output controls the direction of a bidirectional buffer in a buffered system.

LOCK* – Output

LOCK* output indicates that the bus cycle in progress is not to be interrupted. The processor will not service other bus requests (such as HOLD) while LOCK* is active. This pin is configured as a weakly held high input while RESIN is active and must not be driven low.

HOLD – Input

HOLD request input to signal that an external bus master wishes to gain control of the local bus. The processor will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.

HLDA – Output

The HLDA (Hold Acknowledge) output indicates that the processor has relinquished control of the local bus. When HLDA is asserted, the processor has floated its data bus and control signals allowing another bus master to drive the signals directly.

DRQ0, DRQ1 – Input

The DMA Request lines for channels 0 and 1 are asserted high to trigger a DMA. These pins are level triggered and internally synchronized.

UCS* – Output

Upper Chip Select will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, UCS* is configured to be active for memory accesses between 0FFC00H and 0FFFFFFH. During a processor reset, UCS* and LCS* are used to enable ONCE Mode.

LCS* – Output

Lower Chip Select will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. LCS is inactive after a reset.

MCS0* - MCS1* - Bidirectional
MCS2* - MCS3* - Output

The Mid-range Memory Select pins go low when a memory access is made to the mid-range of the memory address space (8K – 512K). The exact address is programmable.

In enhanced mode, the MCS0* pin serves as the PEREQ input. The PEREQ (Coprocessor Request) input signals that a data transfer between the external coprocessor and memory is pending.

Also in enhanced mode, the MCA1* pin serves as the ERROR* input. The ERROR pin indicates that the last numeric coprocessor operation resulted in an exception condition.

The MCS3* pin becomes the NPS* signal in enhanced mode. The NCS* (Numeric Processor Select) pin accesses the Numeric Processor

PCS0*, PCS1*, PCS2*, PCS3*, PCS4* – Output

These pins go low during an access to the defined peripheral area. The specific addresses are programmable.

The PCS5* and PCS6* pins can optionally be programmed to provide latched A1 and A2 signals,

TMROUT0, TMROUT1 – Output

The Timer Output pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.

TMRIN0, TMRIN1 – Input

The Timer Inputs are used either as clock or control signals, depending on the timer mode selected.

INT0, INT1 / SELECT* – Input

Maskable Interrupt inputs will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with INTA0 and INTA1 to interface with an external slave controller.

INT2 / INTA0*, INT3 / INTA1* – Bidirectional

These pins provide multiplexed functions. As inputs, they provide a maskable interrupt that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an interrupt acknowledge handshake signal to allow interrupt expansion.

Pinout

SQFP 80	PQFP 80	PLCC 68	80C186	80C 188
1	64	26	AD0	
2	65	25	AD8	A8
3	66	24	AD1	
4	47		NC	
5	67	23	AD9	A9
6	68	22	AD2	
7	69	21	AD10	A10
8	70	20	AD3	
9	71	19	AD11	A11
10	72		VDD	
11	73	18	VDD	
12	74	17	AD4	
13	75	16	AD12	A12
14	76	15	AD5	
15	77	14	AD13	A13
16	78	13	AD6	
17	79	12	AD14	A14
18	80	11	AD7	
19	1	10	AD15	A15
	2		NC	
20			VDD	
21	3	9	A16	
22	4	8	A17	
23	5	7	A18	
24	6	6	A19 / ONCE	
25			NC	
26	7	5	BHE*	RFSH*
27	8	4	WR*	
28	9	3	RD*	
29	10	2	ALE	
	11		NC	
30	12		VSS	
31	13	1	VSS	
	14		NC	
	15		NC	
32	16	68	X1	
33	17	67	X2	
34	18	66	RESET	
35			NC	
36	19	65	CLKOUT	
37	20	64	ARDY	
38	21	63	S2*	
39	22	62	S1*	
40	23	61	S0*	

SQFP 80	PQFP 80	PLCC 68	80C186	80C 188
	24		NC	
41			VSS	
42	25	60	HLDA	
43	26	59	HOLD	
44	27	58	SRDY	
45	28	57	LOCK*	
46	29	56	TEST* / BUSY	
47	30	55	NMI	
48	31	54	INT0	
49	32	53	INT1 / SELECT*	
50	33		VDD	
51	34	52	VDD	
52	35	51	INT2 / INTA0*	
53	36	50	INT3 / INTA1*	
54	37	49	DT / R*	
55			NC	
56	38	48	DEN*	
57	39	47	McS0* / PEREQ	
58	40	46	MCS1* / ERROR*	
59	41	45	MCS2*	
60	42	44	MCS3* / NPS*	
	43		NC	
	44		NC	
61			VDD	
62	45	43	UCS*	
63	46	42	LCS*	
64	47	41	PCS6* / A2	
65	48	40	PCS5* / A1	
66	49	39	PCS4*	
67	50	38	PCS3*	
68	51	37	PCS2*	
69	52	36	PCS1*	
70	53	35	VSS	
71	54	34	PCS0*	
72			NC	
73	55	33	RES*	
74	56	32	T1OUT	
75	57	31	T0OUT	
76	58	30	T1IN	
77	59	29	T0IN	
78	60	28	DRQ1	
79	61	27	DRQ0	
	62		NC	
	63		NC	
80			VSS	

Note: The PLCC68 package uses the industry standard numbering system where Pin 1 is located in the center of the package. The original Intel part used pin 1 on the corner. The physical signal locations remain the same.

Electrical Specifications

Maximum Ratings

Characteristics	Symbol	Min	Max	Unit	
Supply Voltage	V _{dd}	-0.5	5.5	V	
Input Voltage	V _{in}	V _{ss} - 0.3	V _{dd} + 0.3	V	
Current Drain per Pin	I _{OL}		15	mA	
Operating Temperature Range	Commercial	T _{ac}	0	70	°C
	Industrial	T _{ai}	-40	85	°C
Storage Temperature range	T _{stg}	-55	+150	°C	

DC Electrical Specifications (V_{dd} = 5.0 V +/- 10%, V_{ss} = 0 V, T_a = 0°C to +70°C)

Characteristics	Condition	Symbol	Min	Max	Unit
Supply Voltage		V _{DD}	4.5	5.5	V
Input Low Voltage		V _{IL}	-0.5	0.3 * V _{dd}	V
Input High Voltage		V _{IH}	0.7 * V _{dd}	5.5	V
Output Low Voltage	I _{ol} = 3 mA	V _{OL}	0.0	0.45	V
Output High Voltage	I _{oh} = -2 mA	V _{OH}	V _{dd} - 0.5	V _{dd}	V
Input Hysteresis on /RESIN		V _{HYR}	0.50		V
Input Leakage Current for Pins: AD15:0, READY, HOLD, RES*, CLKIN, TEST*, NMI, INT4:0, T0IN, T1IN, RXD0, BCLK0, CTS0*, RXD1, BCLK1, CTS1*, SINT1, P2.6, P2.7	0 < V _{IN} < V _{DD}	I _{IL1}	-15	+15	uA
Input Leakage Current for Pins: PEREQ, ERROR*	V _{IN} = 0.7 * V _{DD}	I _{IL2}	+/-0.275	+/-7	mA
Input Leakage Current for Pins: A19/ONCE*, A18:A16, LOCK*	Note 1	I _{IL3}	-0.275	-5.0	mA
Output Leakage Current	0.45 < V _{OUT} < V _{DD} Note 2	I _{OL}	-15	15	uA
Supply Current Cold (RESET) 25 MHz 20 MHz 13 MHz	Note 3	I _{DD}		115	mA
	Note 3			108	mA
	Note 3			73	mA
Supply Current in Idle Mode 25 MHz 20 MHz 13 MHz	Note 3	I _{ID}		91	mA
	Note 3			76	mA
	Note 4			48	mA
Supply Current in Powerdown Mode 25 MHz 20 MHz 13 MHz	Note 3	I _{PD}		100	uA
	Note 3			100	uA
	Note 3			100	uA
Output Pin Capacitance	T _F = 1 MHz Note 4	C _{OUT}		15	pF
Input Pin Capacitance	T _F = 1 MHz	C _{IN}		15	pF

Notes:

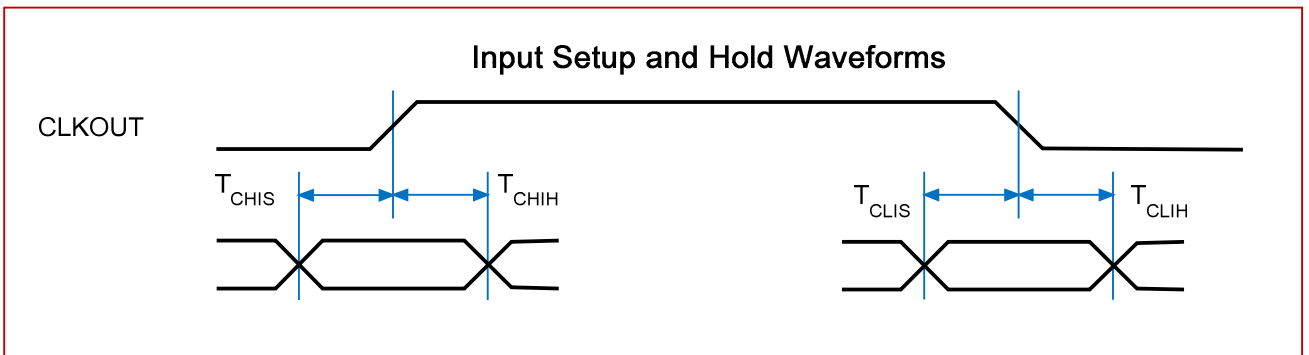
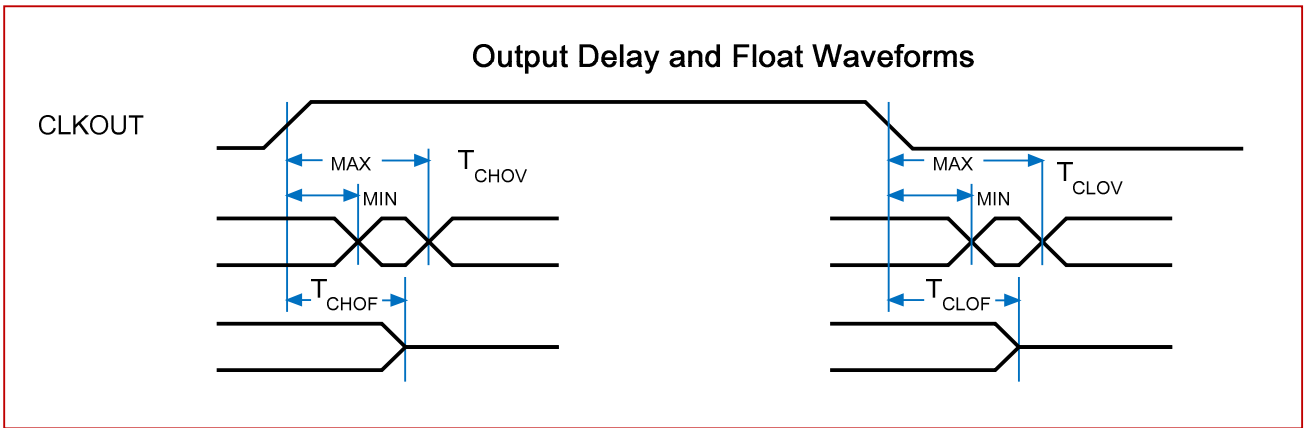
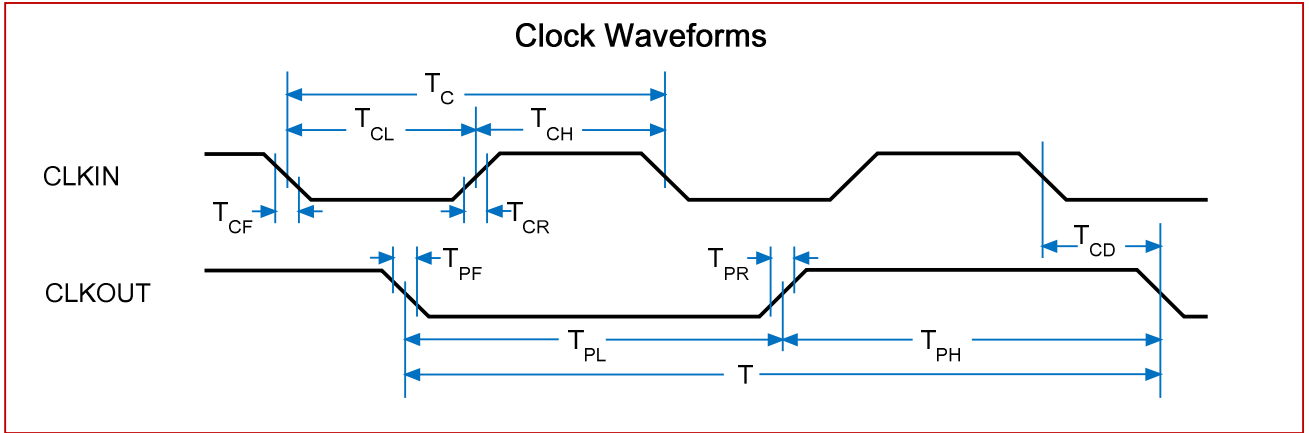
- RD/QSMD, /UCS, /LCS, /MCS0/PEREQ, /MCS1/ERROR, /LOCK and /TEST/BUSY have an internal pullup that is activated during reset.
- Output pins are floated during HOLD or ONCE mode.
- Measured at worst case temperature and V_{dd}, and all outputs loaded.
- Output capacitance is capacitive load of a floating output pin.

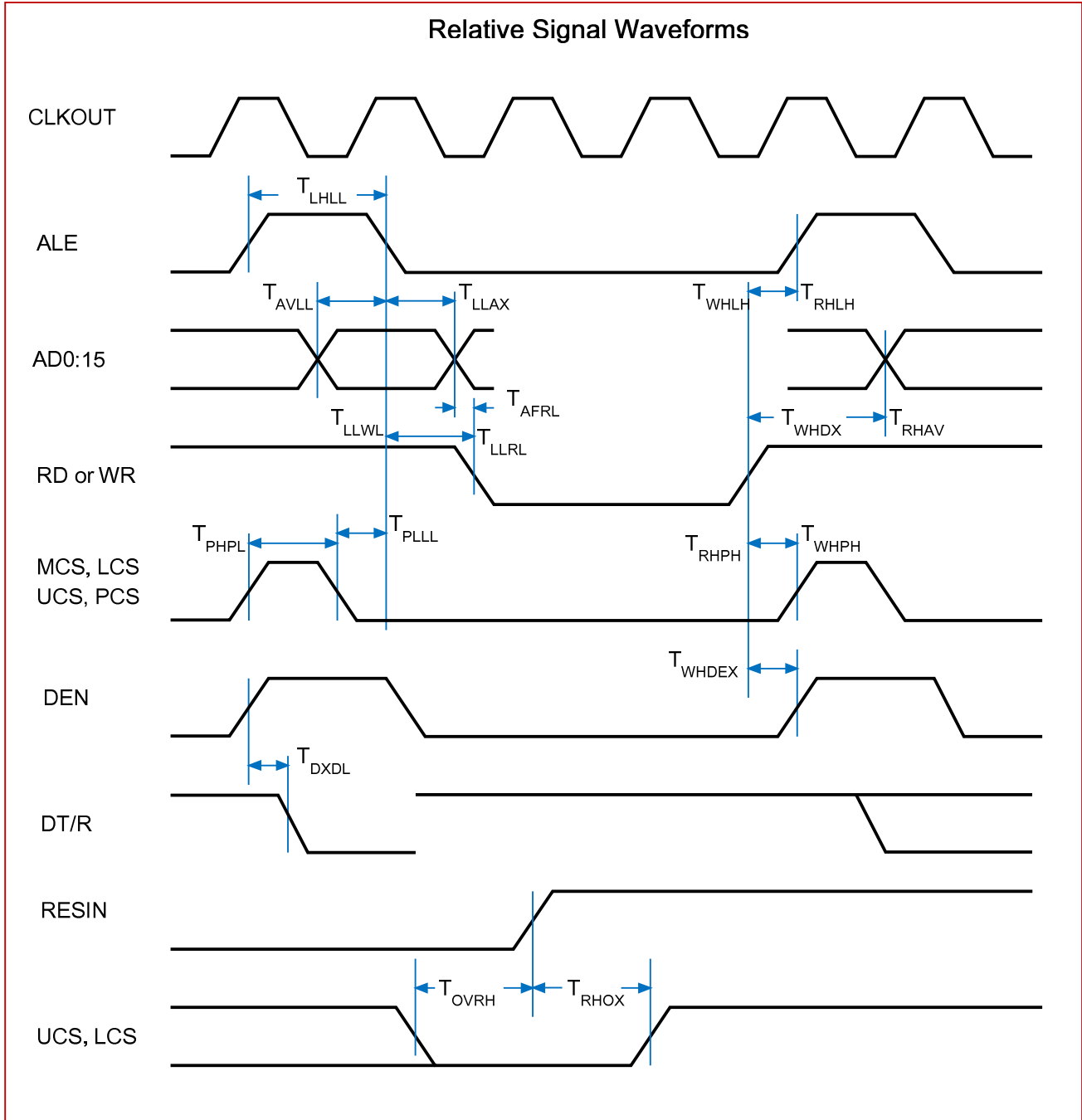
AC Electrical Specifications (V_{dd} = 5.0 V +/- 10%, V_{ss} = 0 V, T_a = 0°C to +70°C)

Characteristics	Note	Symbol	Min	Max	Unit
Input Clock					
CLKIN Frequency	1	T _F	0	50	MHz
CLKIN Period	1	T _C	20		ns
CLKIN High Time	1, 2	T _{CH}	8		ns
CLKIN Low Time	1, 2	T _{CL}	8		ns
CLKIN Rise Time	1, 3	T _{CR}	1	7	ns
CLKIN Fall Time	1, 3	T _{CF}	1	7	ns
Output Clock					
CLKIN to CLKOUT Delay	1, 4	T _{CD}	0	16	ns
CLKOUT Period	1	T		2T _C	ns
CLKOUT High Time	1	T _{PH}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Low Time	1	T _{PL}	(T/2) - 5	(T/2) + 5	ns
CLKOUT Rise Time	1, 5	T _{PR}	1	6	ns
CLKOUT Fall Time	1, 5	T _{PF}	1	6	ns
Output Delays					
ALE, S2:0*, DEN*, DT/R, BHE, RFSH, LOCK, A19:16	1, 4, 6, 7	T _{CHOV1}	3	17	ns
GCS7:0*, LCS*, UCS*, NCS*, RD*, WR*	1, 4, 6, 8	T _{CHOV2}	3	20	ns
BHE*, RFSH*, DEN*, LOCK*, RESOUT, HLDA, T0OUT, T1OUT, A19:16	1, 4, 6	T _{CLOV1}	3	17	ns
RD*, WR*, GCS7:0*, LCS*, UCS*, AD15:0, NCS*, INTA1:0*, S2:0*	1, 4, 6	T _{CLOV2}	3	20	ns
RD*, WR*, BHE*, RFSH*, DT/R*, LOCK*, S2:0*, A19:16	1	T _{CHOF}	0	20	ns
DEN*, AD15:0	1	T _{CLOF}	0	20	ns
Synchronous Inputs					
TEST, NMI, INT3:0, T1:0IN, ARDY	1, 7	T _{CHIS}	8		ns
TEST, NMI, INT3:0, T1:0IN, ARDY	1, 7	T _{CHIH}	3		ns
AD15:0, ARDY, SRDY, DRQ1:0	1, 7	T _{CLIS}	10		ns
AD15:0, ARDY, SRDY, DRQ1:0	1, 7	T _{CLIH}	3		ns
HOLD, PEREQ, ERROR	1, 7	T _{CLIS}	10		ns
HOLD, PEREQ, ERROR	1, 7	T _{CLIH}	3		ns
RESIN (to CLKIN)	1, 7	T _{CLIS}	10		ns
RESIN (From CLKIN)	1, 7	T _{CLIH}	3		ns

Notes:

1. See AC Waveforms for waveforms and definition
2. Measured at VIH for high time, VIL for low time.
3. Only required to guarantee IDD, Maximum limits are bounded by TC, TCH and TCL.
4. Specified for 50 pF load.
5. TCHOV1 applies to BHE, RFSH LOCK and A19:16 only after a HOLD release
6. TCHOV2 applies to RD and WR only after a HOLD release.
7. Setup and Hold are required to guarantee recognition
8. TCHOVS applies to BHE, RFSH and A19:16 only after a HOLD release.
9. AC measurements made with a 50 pF load, at a 50% supply voltage level.
10. Float delay measured with a 3.3K resistor tied to opposite supply, measured after a +/- 0.2V change in voltage level.





Ordering Information

Code	Temperature	Package	Frequency	Replaces
TK80C186XL-25CA	0 to +70	Plastic 68 PLCC – RoHS	25 MHz	N80C186XL25
TK80C186XL-25CB	0 to +70	Plastic 80 PQFP – RoHS	25 MHz	S80C186XL25
TK80C186XL-25CT	0 to +70	Plastic 80 TQFP – RoHS	25 MHz	SB80C186XL25
TK80C186XL-25IA	-40 to +85	Plastic 68 PLCC – RoHS	25 MHz	TN80C186XL25
TK80C186XL-25IB	-40 to +85	Plastic 80 PQFP – RoHS	25 MHz	TS80C186XL25
TK80C186XL-25IT	-40 to +85	Plastic 80 TQFP – RoHS	25 MHz	TSB80C186XL25
TK80C188XL-25CA	0 to +70	Plastic 68 PLCC – RoHS	25 MHz	N80C188XL25
TK80C188XL-25CB	0 to +70	Plastic 80 PQFP – RoHS	25 MHz	S80C188XL25
TK80C188XL-25CT	0 to +70	Plastic 80 TQFP – RoHS	25 MHz	SB80C188XL25
TK80C188XL-25IA	-40 to +85	Plastic 68 PLCC – RoHS	25 MHz	TN80C188XL25
TK80C188XL-25IB	-40 to +85	Plastic 80 PQFP – RoHS	25 MHz	TS80C188XL25
TK80C188XL-25IT	-40 to +85	Plastic 80 TQFP – RoHS	25 MHz	TSB80C188XL25

Contact Information

The TK80C186 series may be ordered directly from Tekmos

Tekmos, Inc.
 4120 Commercial Center Drive
 Suite 400
 Austin, TX 78744

512 342-9871 phone
 512 342-9873 fax
 Sales@Tekmos.Com
 www.Tekmos.com

Revision History

Date	Revision	Description
4/27/09	1.0	Initial release

© 2009 Tekmos, Inc.

Information contained in this publication regarding device applications and the like is intended for suggestion only and may be superseded by updates. No representation or warranty is given and no liability is assumed by Tekmos Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Tekmos' products as critical components in life support systems is not authorized except with express written approval by Tekmos. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights. The Tekmos logo and name are registered trademarks of Tekmos, Inc. All rights reserved. All other trademarks mentioned herein are the property of their respective companies. All rights reserved.

Terms and product names in this document may be trademarks of others.