The Effects of Repeated Refresh Cycles on the Oxide Integrity of EEPROM Memories at High Temperature

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Abstract

Data retention in stored-charge based memories, such as Flash and EEPROMs, decreases with increasing temperature. Compensation for this shortening of retention time can be accomplished by refreshing the data using periodic erase-write refresh cycles, although the number of these cycles is limited by oxide integrity. An alternate approach is to use refresh cycles consisting of a rewrite only cycles, without the prior erase cycle. The viability of this approach requires that this refresh cycle induces less damage than an erase-write cycle. This paper studies the effects of repeated refresh cycles on oxide integrity in a high temperature environment and makes comparisons to the damage caused by erase-write cycles.

The experiment consisted of running a large number of refresh cycles on a selected byte. The control group was other bytes which were not subjected to refresh only cycles. The oxide integrity was checked by performing repeated erase-write cycles on each of the two groups to determine if the refresh cycles decreased the number of erase-write cycles before failure. Data was collected from multiple parts, with different numbers of refresh cycles, and at temperatures ranging from 25C to 190C.

The experiment was conducted on microcontrollers containing embedded EEPROM memories. The microcontrollers were programmed to test and measure their own memories, and to report the results to an external controller. This greatly simplified the hardware setup, since only six wires were required to operate and test the memories of 77 microcontrollers. It also allowed data collection from the microcontrollers while the experiment was in progress.

Data is presented showing that refresh cycles do not have a significant impact on oxide integrity. This result shows that the refresh cycle approach will not degrade the oxide and suggests that it will provide a mechanism to extend data retention at high temperatures without affecting device reliability.

The data also showed a bimodal distribution of the number of erase-write cycles necessary to damage the oxide. Although the cause of this distribution is not yet understood, it may provide an additional means to significantly improve EEPROM reliability through appropriate screening.

Key Words: EEPROM, Data Retention, Oxide Damage, Refresh Cycle

Background

This investigation was driven by Tekmos' development of high reliability, high temperature EEPROM memory. Data retention is a problem at higher temperatures, and can be addressed by either refreshing the data or performing erase-write cycle. [1], [2], [3] It has been previously established that the number of erase-write cycles that a memory can tolerate without oxide damage decreases with higher temperatures. This study was undertaken to determine whether a refresh cycle, a write without erasing first, would also cause oxide damage at higher temperatures.

Another concern was that repeated refresh cycles might cause data corruption in adjacent un-programmed bits. This phenomenon is also known as write disturb. This problem, if present, would likely be due to the physical layout of the EEPROM cell. A second study was made to determine the maximum number of refresh cycles that could be performed without adjacent data corruption.

Experimental Procedure

For a given device and temperature, an EEPROM byte was given write-erase cycles until it failed. Then a second byte was given a high number of refresh cycles before subjecting it to the same test of repeated write-erase cycles until failure. This was repeated with a number of units and at various temperatures.

In the data corruption study, we gave a byte multiple write cycles, and verified that the correct data was read from the byte. This was repeated until either failure, or until it was decided to end the experiment

Setup

The tests were performed on the Tekmos TK68HC11E1 microcontroller which contains 512 bytes of EEPROM. All devices come from the same manufacturing lot. Prescreening included subjecting each microcontroller to a 260C, 24 hour data retention bake prior to assembly.

The microcontrollers were grouped 77 to a board, and configured so that each processor was individually addressable. The TK68HC11 architecture has a bootstrap mode that allows the downloading of programs into RAM, making it easier to conduct different experiments, and to collect continuous data from the microcontrollers while they were in the oven. It also allowed soldering the parts onto the burn-in board, significantly reducing the overall cost and improving the experiment's reliability.

It should be noted that EEPROMs in the microcontrollers are slow to program and to erase, taking 10 ms to erase a byte, and another 10 ms to write data back into it. This makes it impractical to exercise more than one byte per part at a time since a million cycles takes over 5 hours to complete. Testing a large number of parts in parallel compensated for this.

Since a given experimental run could take over a week to complete, there was some risk of losing data in the event of a power failure or an interruption of the experiment for other reasons. To protect against data loss, the current cycle count was stored in EEPROM every 10,000 cycles.

Initial Oxide Burnout Testing

Parts were tested for oxide burnout at 25C, 75C, 125C, 150C, 175C, 185C, and 190C.

For temperatures of 125C and below, a distinct bi-modal distribution was observed in the number of erase-write cycles it took to damage a part. While 60% of the bytes failed as anticipated, the other 40% of the bytes did not fail within the experimental limits. One board was set aside and to determine how many erase-cycles it would take to destroy all of the bytes. That experiment was terminated after running over 100 million erase-write cycles without inducing oxide damage. The bimodal distribution was greatly reduced at 150C, and was not observable at 175C.

Because design constraints require a guarantee of a minimum number of erase cycles, the choice was made base the data analysis on the lower mode of the distribution.

Figure 1 shows the distribution of the number of erase-write cycles required to induce damage in our EEPROM at 25C. This graph clearly shows the bi-modal distribution.

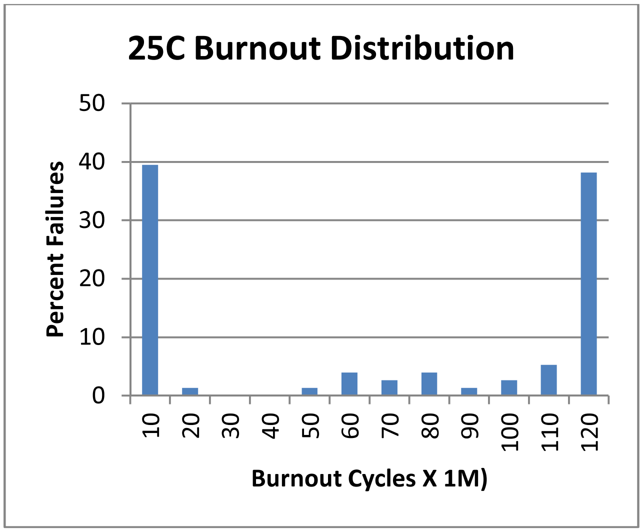

Figure 1

Figure 2 shows the reduction in the mean number of erase-write cycles necessary to induce damage as a function of temperature. This has been previously reported. [1] Note that there are other studies that suggest that the number of erase-write cycles required to induce damage increases with temperature [4], but that was not observed in the data from these experiments. Those studies concentrated on temperatures < 0C, and did not cover higher temperatures.

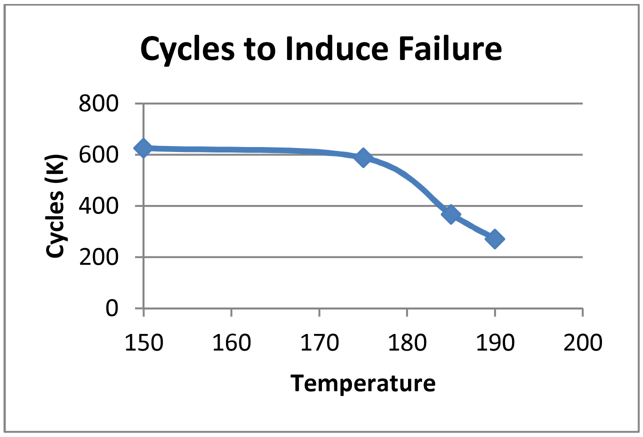

Figure 2

Figure 3 shows the distribution of the number of erase-write cycles necessary to damage oxide at 190C.

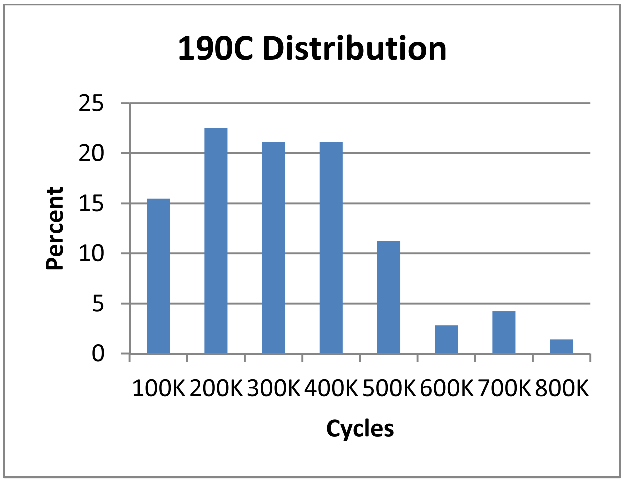

Figure 3

Refresh Cycle Testing

A refresh cycle consists of writing the existing data back into the part. The concept is to replenish charge that may have leaked away. There are two concerns with a refresh cycle. The first is that the high voltages associated with refresh may damage the part. The second concern is that repeated refreshes may cause adjacent un-programmed bits to become programmed.

The parts were subjected to 1 million refresh cycles, and then an oxide burnout test was conducted to see if this had reduced the number of erase-write cycles the oxide could tolerate before failure.

Table 1 shows the means and standard deviations for the number of erase-write cycles necessary to induce oxide damage. While the means for the refreshed parts tended to be slightly higher than the control, they were well within the standard deviations.

Refresh Cycle Results				
	No Refresh		1M Refresh	
Temp	Mean (K)	Std Dev (K)	Mean (K)	Std Dev (K)
150°C	626	217	662	241
175°C	588	162	625	206
185°C	344	203	301	144
190°C	217	161	420	240

Table 1

Refresh Induced Data Corruption

An investigation was performed to see if there was a limit to a maximum number of refresh cycles that could be performed before corruption of the non-programmed bits. This is also known as write disturb.

Several EEPROM manufacturers have warnings about possible data corruption resulting from adjacent writes. This is likely a design and layout related phenomena. None the less, it was investigated to insure that it is not present in the Tekmos EEPROM.

Each byte was subjected to repeated writes of a 55h pattern, and then read to verify that the data was still 55h. This was repeated until the experiment terminated. Five experiments were run at 175C. Each was terminated due to time constraints. No write errors were ever observed. The results are in Table 2.

Repeated Refresh Cycles		
Exp.	Cycles	Comment
1	4.9 M	No damage
2	6.6 M	No damage
3	7.3 M	No damage
4	7.3 M	No damage
5	39.7 M	No damage

Table 2

Circuit Performance

Supplemental checks were performed to insure that the microcontrollers were operating properly.

Figure 4 shows the supply current for a board of 77 microcontrollers as a function of temperature. The leakage was not noticeable below 185C. This was as expected.

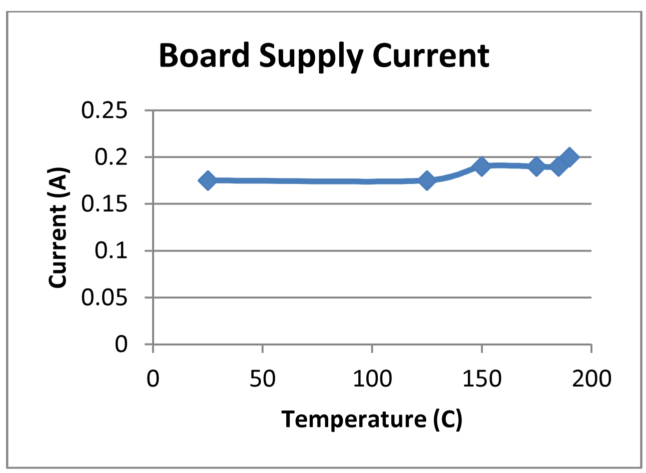

Figure 4

Each of the Tekmos microcontrollers has a reliability monitor built into it. This monitor contains a number of ring oscillators designed to detect common reliability issues such as hot electron injection or threshold shifts. The frequency was monitored to insure that the circuit operation was not being degraded by any factor other than temperature. Specifically, it was important to insure that junction leakage was not a factor.

Figure 5 shows the ring oscillator frequencies as a function of temperature. The decline in oscillator speed with temperature was as expected.

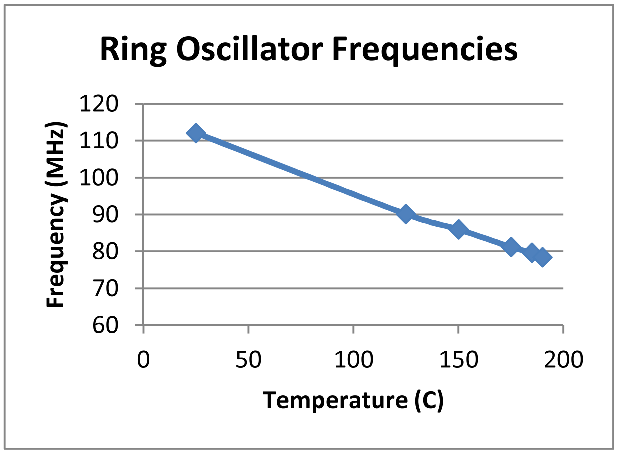

Figure 5

Conclusions

No degradation of oxide strength with repeated refresh cycles was seen. No data corruption with repeated writes was observed.

This indicated that use of a refresh cycle to restore charge in EEPROMs is a valid technique for combatting data retention issues at high temperature.

Future Research

There was a hint that refresh cycles at higher temperatures may actually be beneficial to oxide integrity. This needs to be investigated further.

The bimodal oxide distribution at lower temperatures was an unexpected phenomenon. Finding a means to nondestructively test for it could provide a higher reliability memory.

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